

Final Report — Phase I

FEASIBILITY STUDY FOR RELIABLE MAGNETIC CONNECTION SWITCH

By: E. K. VAN DE RIET D. R. BENNION J. M. YARBOROUGH

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SR I Project 5669

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COMPUTER TECHNIQUES LABORATORY

J. D. NOE, EXECUTIVE DIRECTOR
ENGINEERING SCIENCES AND INDUSTRIAL DEVELOPMENT

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ABSTRACT

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The goal of the investigation described here is to determine the feasibility of using magnetic circuits in a section of a computer requiring very high reliability. The circuits provide the gating and voting functions required to switch signals from redundant subsystems to a central information bus.

Shift registers using multiaperture magnetic cores are used as a means of selecting subsystems. The minor apertures are used as transformers which will pass signals when the core is set and will block them when cleared. The position of the ONE in the register determines the selection of a particular subsystem by unblocking the aperture that is coupled to the selected subsystem output. The position of the ONE in the register is shifted once along the register to select the next subsystem each time the one in use fails.

Voting circuits required in this application use a technique where the three signals on which a vote is to be taken are each coupled to an associated core. These three cores are coupled to each other with a series winding which also links a fourth core. This additional core cancels the mmf induced in the common winding by any single core. The effect of more than one core switching at a time will be too large to be nullified by the cancelling core and will produce an output. The voting is thus accomplished since two or more cores switching represent a majority of the outputs. If only one switches, it is a minority and its effect is nullified by the cancelling core.

The drivers for the magnetic circuits are redundant semiconductor circuits.

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I INTRODUCTION

This report describes an investigation of the feasibility of using magnetic circuits in a switching application that requires high reliability. The application is a switch for connecting the central information bus of a computer to its memory and arithmetic unit subsystems. These subsystems are redundant and the switch connects the central information bus to the succeeding operable subsystem when one or more of those in use fail.

The main purpose of the report is to describe a number of magnetic circuit approaches to the problem and to evaluate them relative to each other on the basis of reliability, performance, power dissipation, and cost.

Estimates are given of the number of integrated semiconductor modules required for an integrated semiconductor version of the switch, and a comparison is made with the number of semiconductors required for the drivers of the magnetic switches.

II CONNECTION SWITCH FUNCTION

There are three identical connection switches in the computer system being considered here. One is for the arithmetic units and two are for the memories. The discussion here will refer to the arithmetic unit switch, with the understanding that there are two more identical switches for the memories.

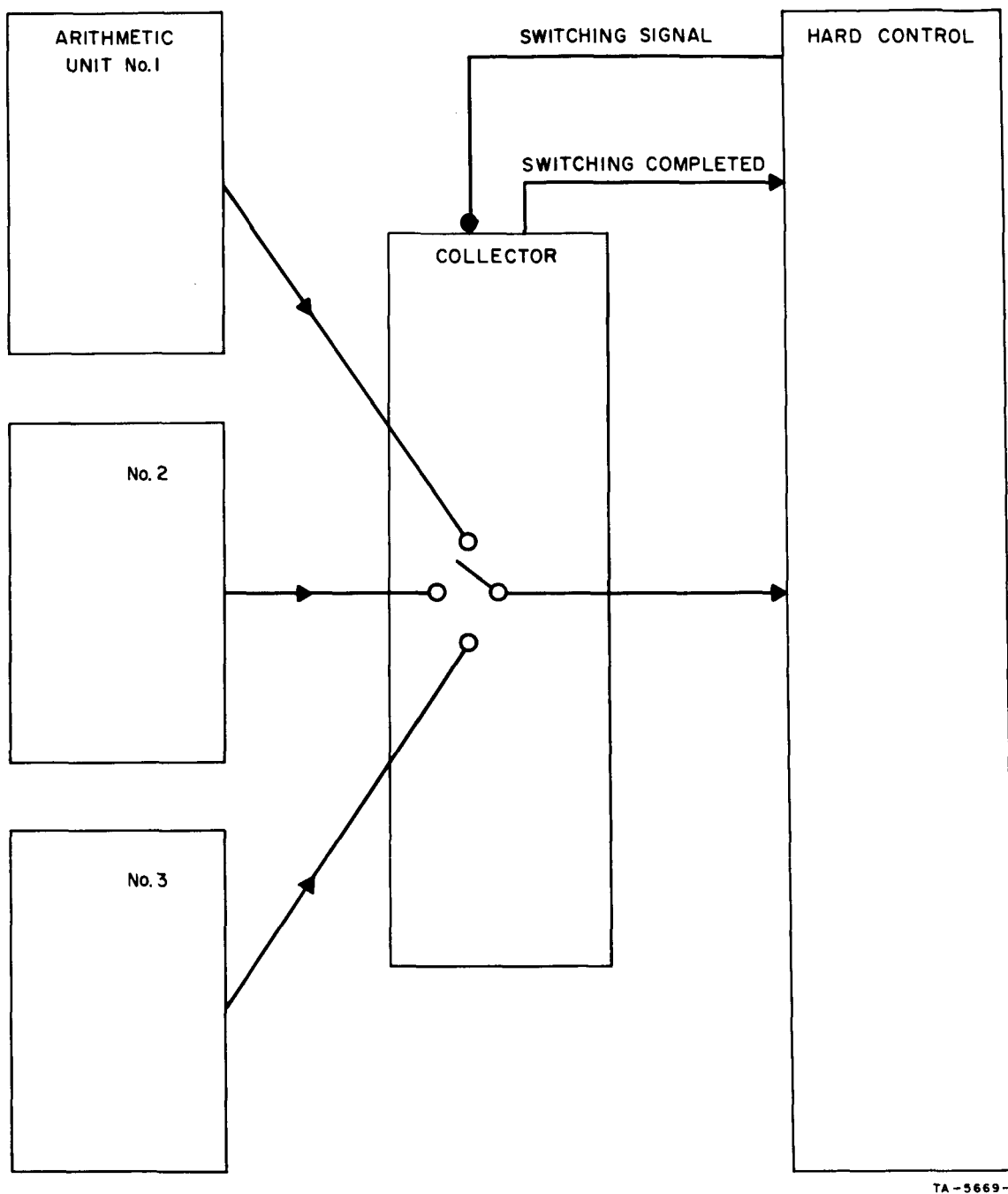
The connection switch is made up of two independent switches called the Collector and Distributor. The Collector gates information from one of the three arithmetic units at a time to the Hard Control. The Distributor distributes the information from the Hard Control to all of the Arithmetic Units at once.

A. Collector

A simplified block diagram of the Collector is shown in Fig. 1. A switching signal from the Hard Control causes the Collector to switch to the next Arithmetic Unit.

The switch is initially reset to connect Arithmetic Unit 1 to the Hard Control. This position is held until Arithmetic Unit 1 fails, at which time the Hard Control puts out a switching signal to the Collector to change to the next Arithmetic Unit, which in this case is Unit 2. When Unit 2 fails, Unit 3 is connected in the same way.

Each Arithmetic Unit has six inputs and six outputs. The Hard Control has six inputs and six outputs, each of which is triply redundant. The Hard Control also has switching outputs that are triply redundant. With the Cyclic type of Collector it has one switching output, and with the Selector type of Collector it has three. These two types of Collectors will be explained later. A somewhat more complete block diagram of the Collector with labels on the inputs and outputs of the Arithmetic Units and Hard Control is shown in Fig. 2. Only two of the six lines from each Arithmetic Unit to the Collector are shown to prevent the drawing from being too cluttered. The outputs



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FIG. 1 SIMPLIFIED BLOCK DIAGRAM OF THE COLLECTOR

of the Arithmetic Units are labeled A10-1 through A10-6. The A1 indicates Arithmetic Unit Number 1, the 0 indicates "output," and the digit after the hyphen indicates the number of the output. The input labels are the same except that the 0 is replaced by an I.

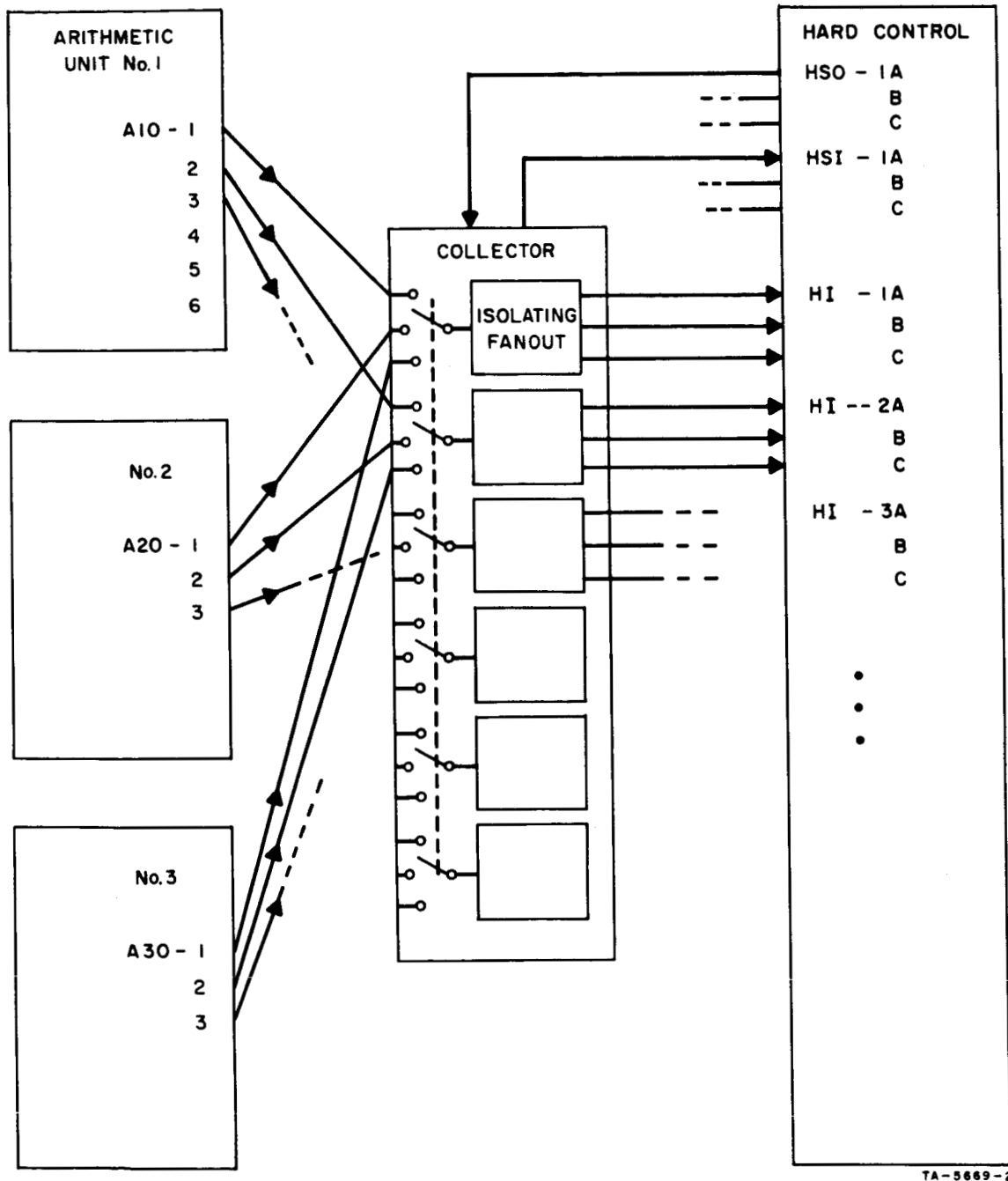


FIG. 2 DETAILED BLOCK DIAGRAM OF THE COLLECTOR

The outputs of the Hard Control, which is the name given to the central information bus, are labeled HO-1A through HO-6C. The HO indicated "Hard Control Outputs." The number after the hyphen indicates

the number of the output and the letters A, B, and C relate to three redundant channels of each output.

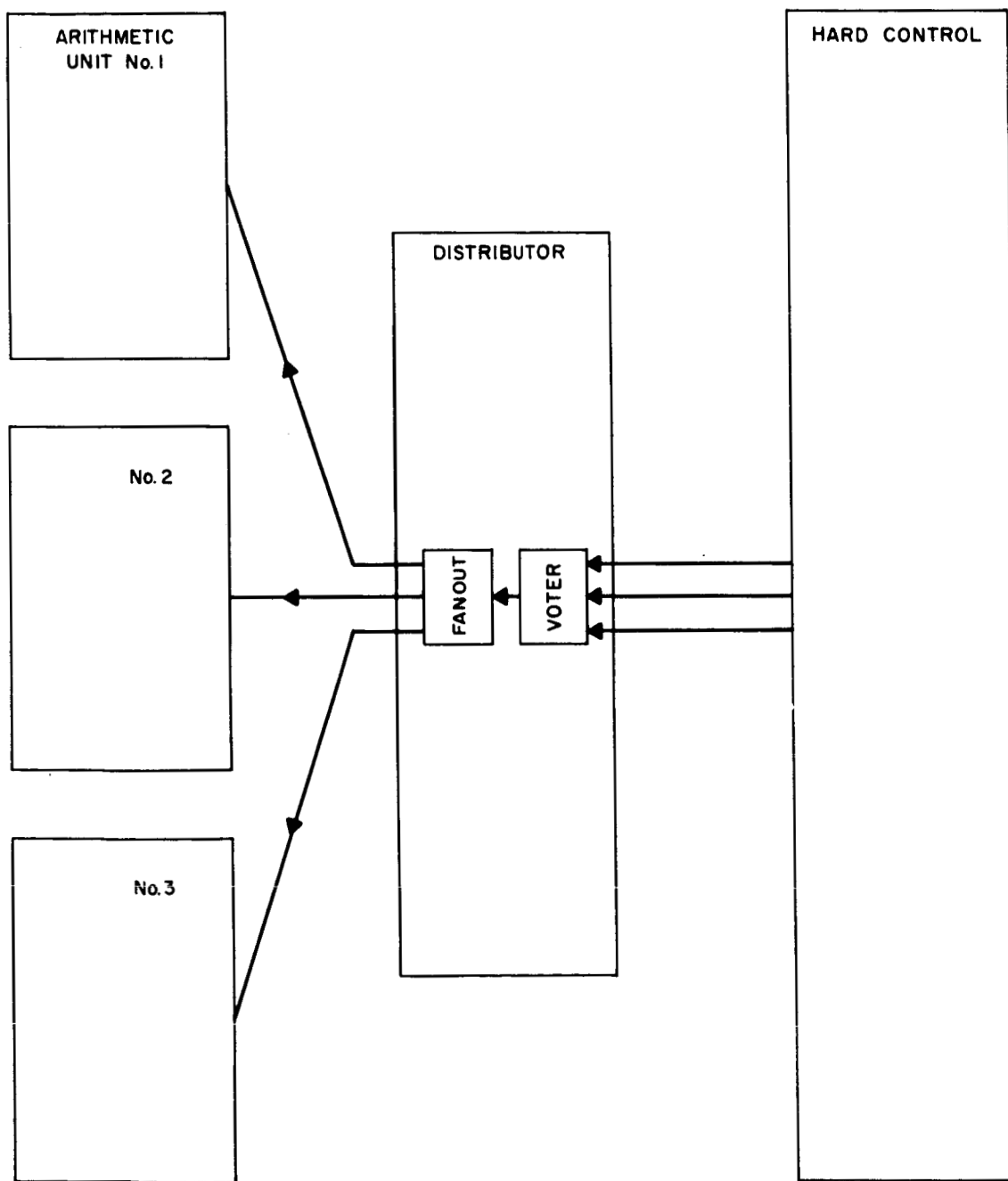
Again the inputs are indicated with an I instead of an O.

The switching inputs and outputs have an SI or an SO following the H.

B. Distributor

A simplified block diagram of the Distributor is shown in Fig. 3. The function of the Distributor is to take a vote from the redundant output trio and transmit the result to all three Arithmetic Units. It is assumed that power will be applied to only one Arithmetic Unit at a time, but even if it is applied to all of them, the signals entering the spare units will not cause any problems since the Collector prevents them from transmitting any information out.

The more detailed block diagram of Fig. 4. shows all of the terminals but leaves out some of the interconnecting lines to prevent the drawing from being too cluttered. An alternative arrangement with the voters after the fanout gives higher reliability at the cost of three times the number of voters. This arrangement will be described in more detail in a later section where the specific circuits are explained.



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FIG. 3 SIMPLIFIED BLOCK DIAGRAM OF THE DISTRIBUTOR

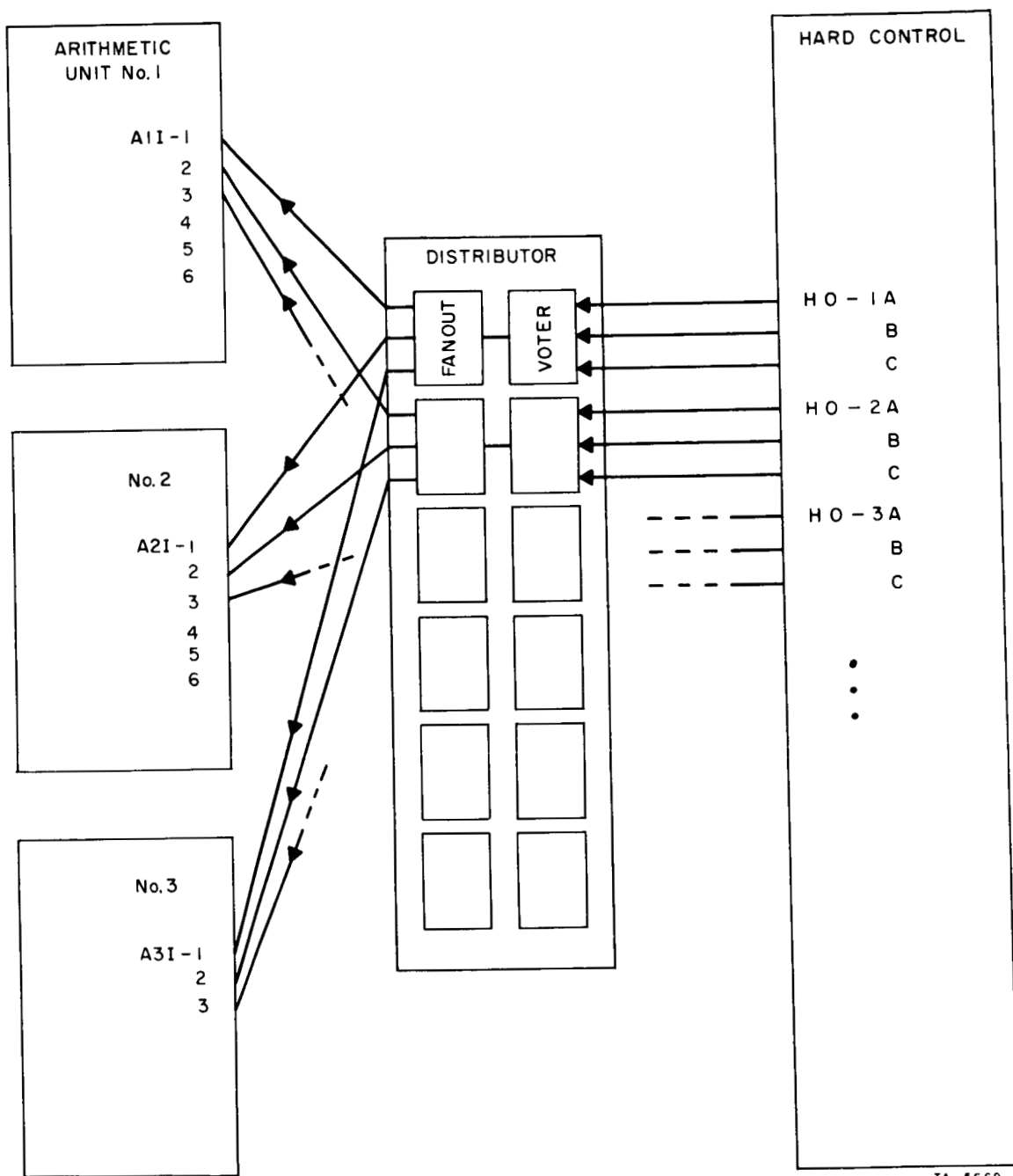


FIG. 4 DETAILED BLOCK DIAGRAM OF THE DISTRIBUTOR

III CYCLIC COLLECTOR

A. Introduction

The Collector designs described in this section are based on the premise that magnetic core-wire circuits are uniquely ultrareliable, in the sense that redundancy is not needed in order for reliability to be comparable to that of surrounding redundant circuits. Based on this premise, only core-wire portions of the switch are allowed to be non-redundant. Since the core-wire circuits require position-changing drivers including components other than cores and wire, these drivers must be redundant.

It would be most desirable for these drivers to have redundant replicas that could be switched in and out by the switch itself. This has not been shown to be impossible, but no complete ideas for accomplishing this feature are presently available. The present designs are based on triple redundancy with voting.

Given the triply redundant drivers, there are two main alternatives for organizing the switch. First, the switch proper may also be triply redundant, with each replica feeding one of three inputs to the Hard Control, so that no voting is required within the Collector Switch. Second, the switch may be nonredundant, requiring a voting interface between drivers and core-wire switch, and fanout circuitry from switch to Hard Control. In considering the second case, we have found ways to accomplish the voting and fanout functions with core-wire circuits, and hence these interface circuits themselves need not be redundant.

The cyclic nature of the Collector implies a shift register. There are many known schemes for core-wire registers, but in terms of drive and temperature tolerances and ease of design, none are superior to the scheme known as MAD-R. Transfer speed is very low (order of 1/2 msec when design is for maximum tolerances), but this is apparently well within any time requirement for changing switch position.

The MAD-R scheme employs multiaperture cores, and extra minor apertures in the shift-register cores are used for switch elements. The basic switching techniques described here make use of one bit-length of register for each switch position. Storage of a "1" corresponds to a closed switch position, and hence the register always stores only a single "1" since only one position is closed at once.

The approach used below in describing the triplet (redundant) and singlet (nonredundant) switches is to treat straightforward realizations based on presently available components. In describing the two main alternatives, we treat the overall redundant switch first, then the nonredundant one, and then the shift-register circuit used three times in the former and once in the latter. Next the details of information wiring for the two switches are considered, and finally the voting circuit required for the latter is described. Schematics are shown for straightforward realizations based on present components and known design techniques. Some possibilities for greater economy of components and power are described in terms of variations from the circuits illustrated.

After description of the circuitry, tabulations of estimated drive requirements, performance, dimensions, and component counts are provided.

Finally, estimates are made of some of the improvements potentially obtainable by design of cores specifically for this application.

B. Redundant Switch

The redundant switch, along with the associated peripheral equipment, is shown schematically in Fig. 5. Although this switch uses more components than the nonredundant one, it is the more straightforward of the two and hence is treated first.

Each of the three registers shown is a three-bit MAD-R register, with end-around loop for circulating the binary pattern that controls switch position. This pattern consists of a single "1" followed by two "0's" set into corresponding bits of each register by the Preset Driver. The independent register drivers (RD) each consist of two Advance



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Drivers and one Prime Driver for supplying the necessary sequence of four drive pulses: ADV E, Prime, ADV O, Prime. This drive sequence is triggered simultaneously for all three columns by the three lines from Hard Control (provided no failures have occurred in Hard Control or the Switch). At the end of the sequence, signals are fed back on three lines, as indicated, to signal "End-of-Shift" to Hard Control.

The signals (six assumed) from the active arithmetic unit (AU) must be connected through the corresponding portions of all three registers, as indicated in full for AU_1 , in Fig. 5. These signals must be amplified by Information Drivers (ID) in order to drive minor apertures of multiaperture cores in the registers. The outputs of corresponding "terminals" for all three positions of a register are combined in an OR circuit to feed an input to the Hard Control. Three such connections feed a triplet of inputs, as illustrated in Fig. 5.

Voting is assumed to take place only in the Hard Control. Thus, failure in any one switch column--whether in the trigger from Hard Control, the Register Driver, or the Register itself--will result in single errors to Hard-Control input triplets. These errors can be voted out, but failure in two columns would of course amount to complete breakdown of the switch.

C. Nonredundant Switch

The nonredundant switch is illustrated in Fig. 6. In comparison to the previous switch described, three registers have been replaced by one, but two additional components--the Register Voter and a set of Fanout circuits--are required.

Even single failures, not only in the Register but also in the Register Voter, cannot now be tolerated, but these circuits can be entirely core-wire in nature, as will be illustrated below. In principle, some types of single failures could be tolerated in the fanout circuits, but a "short" could affect the other Hard Control inputs in the same triplet. Hence this circuit should also be core-wire or else use redundant components.

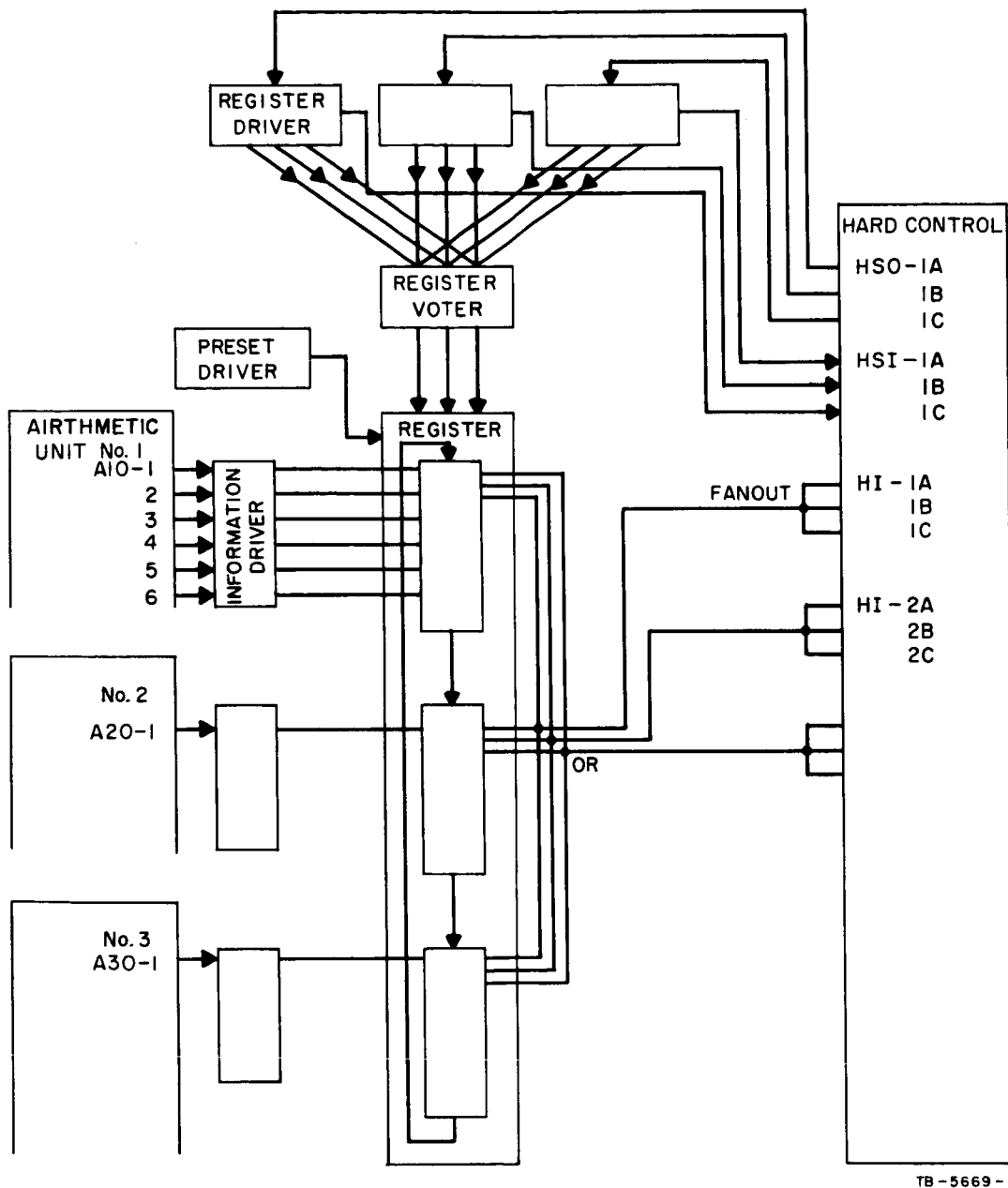


FIG. 6 BLOCK DIAGRAM OF NONREDUNDANT COLLECTOR

The only apparent advantage of the nonredundant switch is the use of one-third the number of shift-register bits, but this is partly balanced by the extra components required for voting and fanout. It might appear that register drivers could be lower-powered (three units driving only one register), but the opposite is true. As will be

shown later, the Voter operates by cancelling the effect of one of each three drivers during any one pulse period. Thus if only two operate, any one driver must carry the load of driving the register. Further, because of losses in the Voter, each driver must be somewhat higher-powered than those that are driving registers directly as in the case of the redundant switch.

The other main disadvantage for the present switch is that the Voter circuit, though already substantially tested in the laboratory for this project, needs more careful, detailed design; and this process interacts with design of the register.

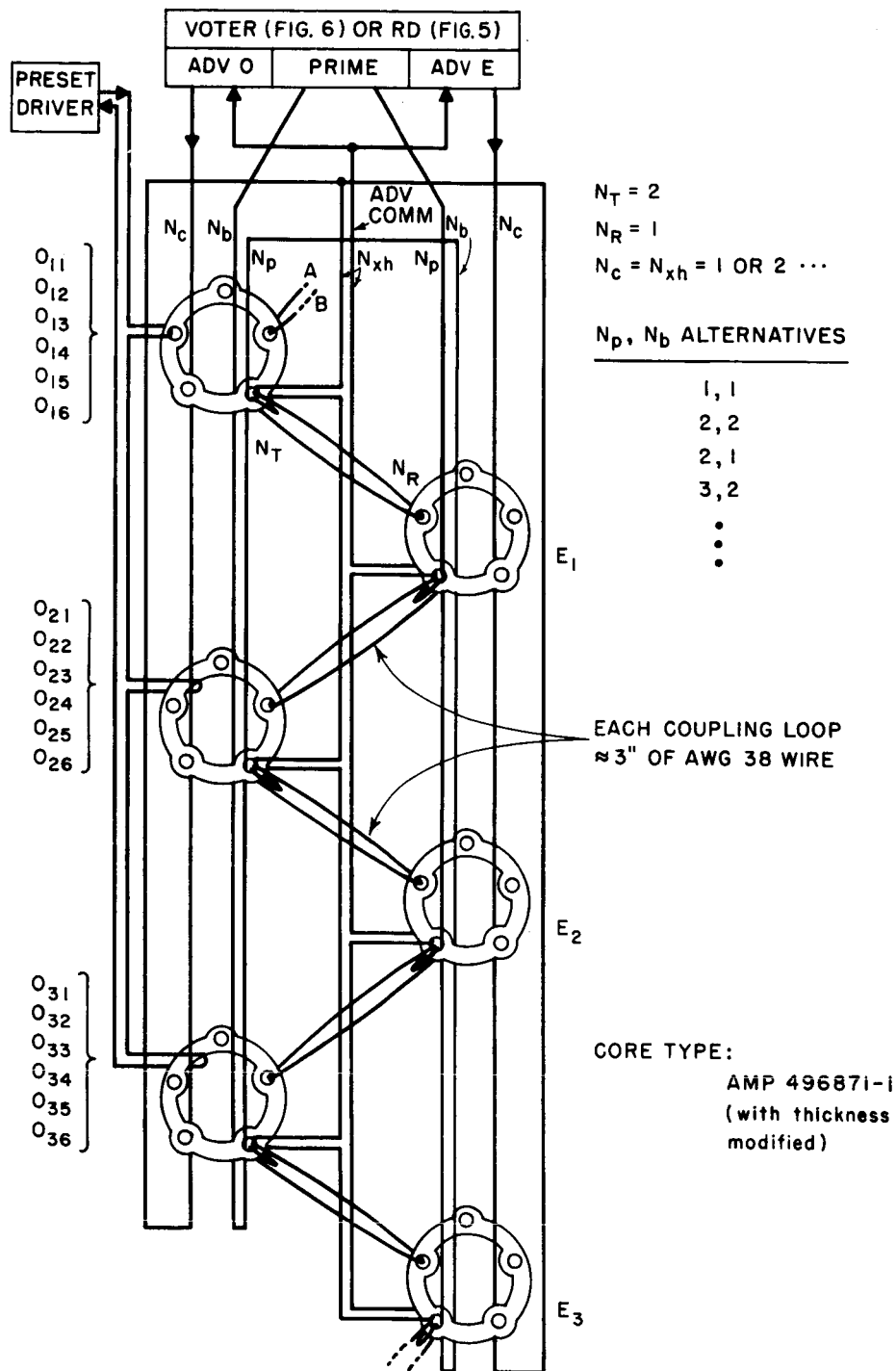
There should not be a significant difference in requirements on the Information Drivers, since the reduced requirement of driving minor apertures in one register only will be about balanced by the increased requirement of indirectly driving fanout circuits.

D. Register Circuit

A schematic of the Register circuit is shown in Fig. 7. This schematic can be viewed as practically an assembly drawing also, except that the cores are generally mounted on edge to facilitate the "straight-through" wiring implied by the drawing. Although having more minor apertures than needed for this application, the core type illustrated is not only a good general-purpose type, but the best available for the switch at this time.

The register shown here may be viewed as either the first of three for the redundant switch or as the single one for the nonredundant switch. However, in the latter case (as will be seen later, in Fig. 10), the Advance Common line actually links through the Prime portion of the Voter before dividing to return to the two Advance portions.

The register cores are divided into an Odd (O) set and an Even (E) set, each driven by an Advance Driver and in common by a Prime Driver. The pulses occur in the sequence Advance O (transferring from O to E cores), Prime (priming E cores), Advance E (transferring from E to subsequent O cores), Prime (priming O cores). Both Prime pulses are



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FIG. 7 SCHEMATIC OF REGISTER

applied identically, but the first one does not affect the O cores (due to their being in the Clear or Blocked state), and the second one does not affect the E cores.

The Preset drive line is shown linking the O cores in such a way as to set the first stage, O_1 , and clear the other two stages, O_2 and O_3 . (For the redundant switch, this same line would link the other two registers in the same way.) The effect of this Preset is to close the first switch position and assure that the other two are open. After one drive sequence (Adv O, Prime, Adv E, Prime), only the O_2 stage will be set, and hence the switch will have been advanced one position.

In this scheme, the E stages serve only as intermediate transfer positions and are not coupled by any information lines. Each information channel (not shown in Fig. 7) must be coupled via a minor aperture of an O core. Assuming six channels as we do here, and assuming only one channel per core, each O stage must consist of six stacked cores (Cores O_{11} , O_{12} , O_{13} , O_{14} , O_{15} , O_{16} , for Stage O_1). These cores are linked in common by register drive lines and coupling loops, but separately by information lines.

Some typical quantitative values for register circuit design are indicated in Fig. 7. The values chosen for the combination N_p , N_b depend on Prime driver design (e.g., rate of rise of the Prime pulse) and on degree of emphasis on minimizing turns. In general, $N_c = N_{xh} = N$, with the value of N depending on current level versus voltage level, and number of turns. At this stage, there is no reason to consider other than 2, 1 for the coupling-loop turns ratio N_T , N_R . As for the core, present ones are nominally 0.060 inch thick and have 0.3 volt- μ sec flux capacity. These can be readily ground down to 0.020 inch thick in order to provide the 0.1 volt- μ sec cores for the O stages. The E stages should consist of two standard cores stacked, unless doubly thick cores can be readily obtained.

E. Information Wiring for the Redundant Switch

The details of the information wiring for the redundant switch are shown in Fig. 8, where the six stacked cores, for not only the O_1 stage but also the O'_1 and O''_1 stages of the other two registers, are shown in

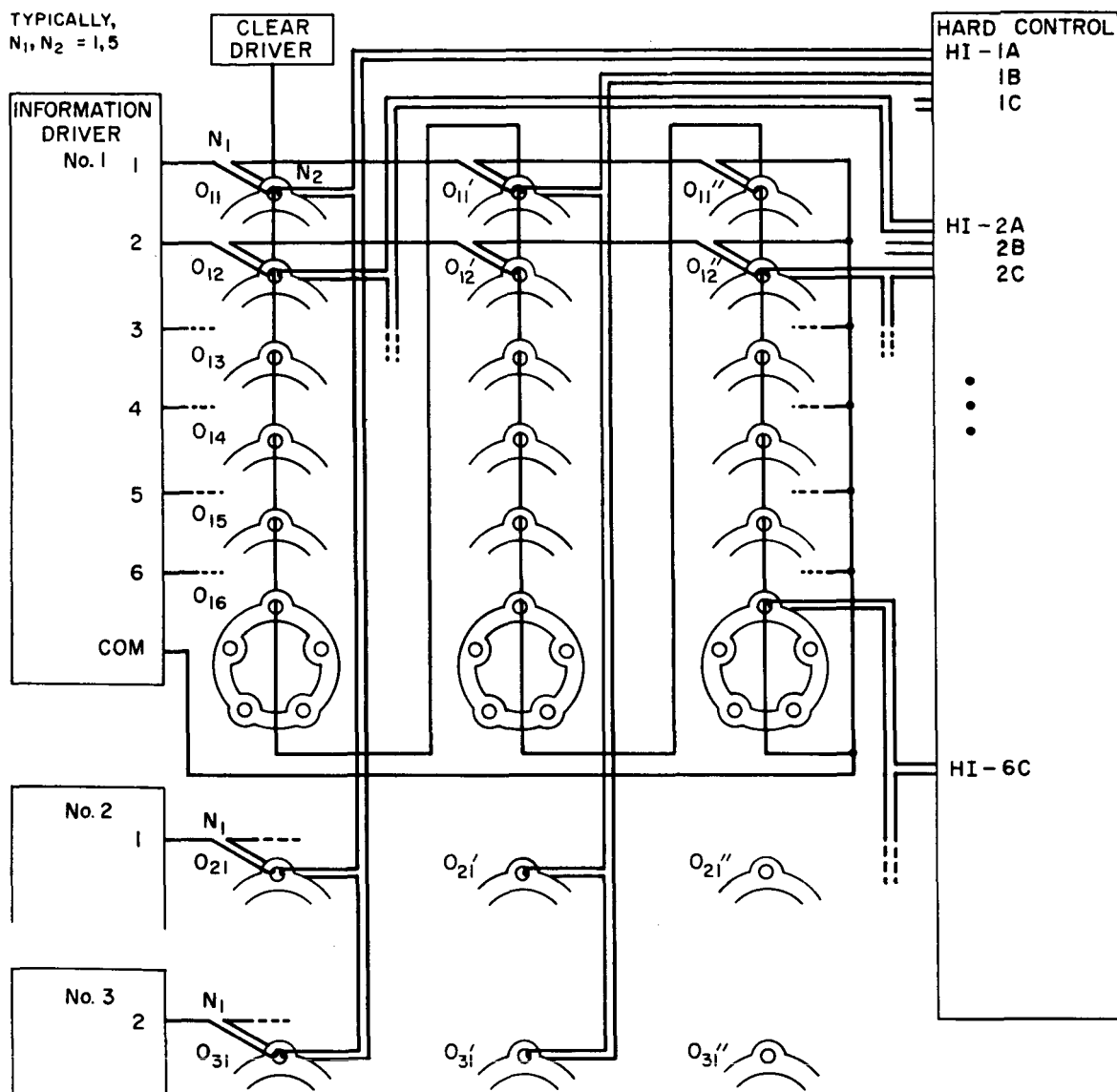


FIG. 8 INFORMATION WIRING FOR REDUNDANT COLLECTOR

spread-out fashion. It can now be seen that the way each output from an information driver controls three switch points (as was indicated in Fig. 5) is to link three minor apertures in series (e.g., Lines 1 and 2 from ID_1 in Fig. 8). Flux is switched around the minor apertures only if the information output on the line is a "1," but any flux so switched must be reset prior to the next information pulse (which occurs one microsecond after the previous one). This Reset function may be accomplished with a single drive line linking all cores in the first 0

stages of each register, as shown. An alternative method would be for each information driver to supply bipolar pulses (a positive pulse followed by a negative one).

The OR function output for corresponding cores in the three switch positions is also accomplished with a series winding coupled to the appropriate Hard-Control input (e.g., as shown for Cores O_{11} , O_{21} , and O_{31}). Enough other examples are shown in Fig. 9 to illustrate the principle of the complete wiring scheme.

An alternative to the common return for the six lines from ID_1 would be to return each one individually to its own section of the driver unit, perhaps resulting in lowered noise generation.

For cores of the flux capacity suggested (0.1 volt- μ sec), it is estimated that a turns ratio of $N_1:N_2 = 1:5$ would be appropriate for providing adequate triggering voltage and tolerances for driving the Hard Control.

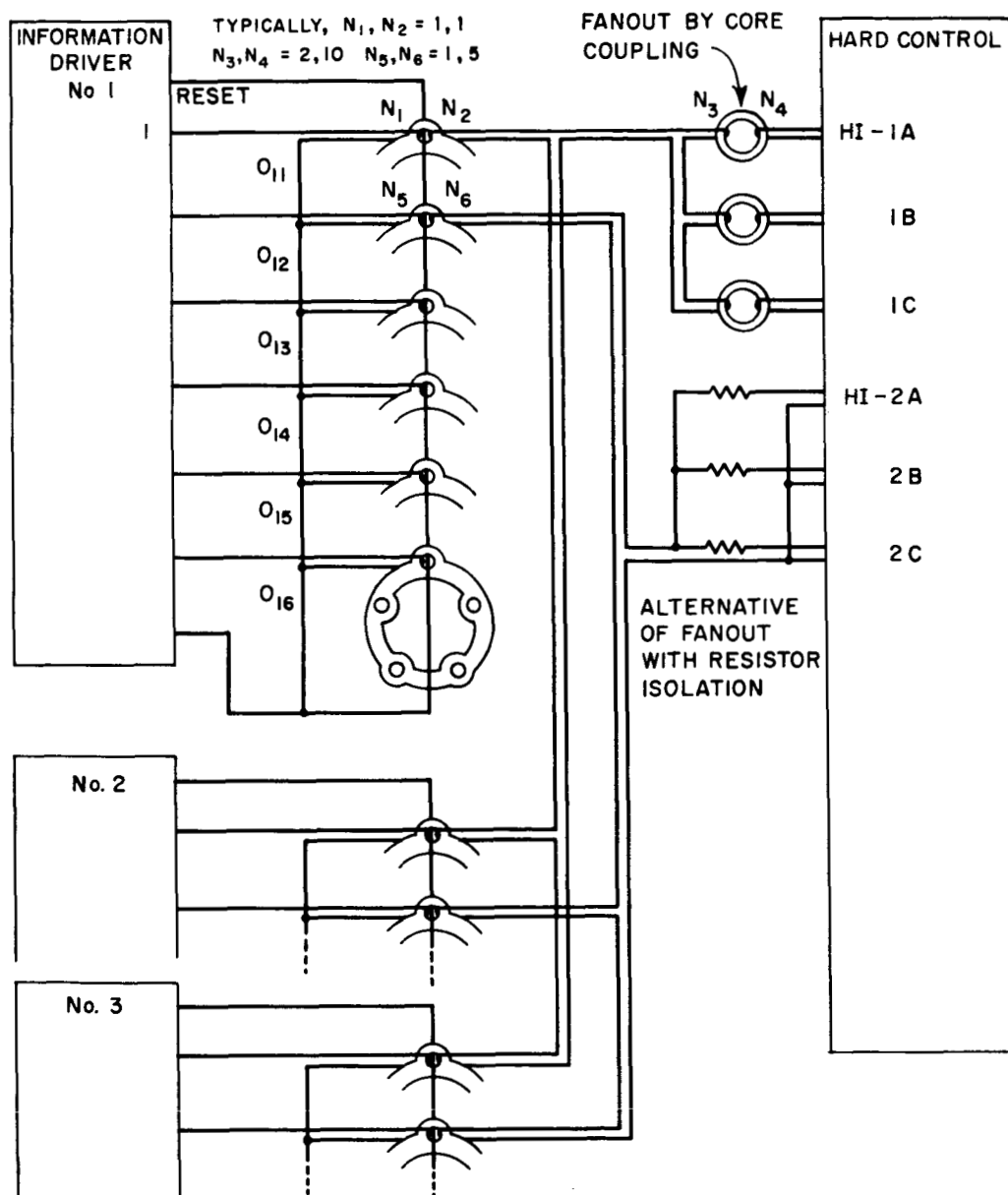
F. Information Wiring for the Nonredundant Switch

From Fig. 9, we see that the input information for the nonredundant switch is the same as for the previous one, but now linking only one register instead of three. But the output circuitry, besides incorporating the OR functions, must now also provide for fanout.

Two alternatives for accomplishing the Fanout function are shown in Fig. 9. A necessary condition is that each input to the Hard Control be well isolated from its two mates in order that a failure in one does not prevent operation of the other two. The first (upper) alternative illustrated in Fig. 9 achieves isolation by means of coupling through toroidal cores.

The second alternative simply uses resistors for isolation. To be consistent with the principle of having no nonredundant components other than cores and wire, each of these resistors should be replaced by an appropriately redundant set of the same.

The first alternative has the advantages of separate windings to the three inputs in a trio, and of allowing the step-up turns ratio



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FIG. 9 INFORMATION WIRING FOR NONREDUNDANT COLLECTOR

($N_3:N_4 = 1:5$) to be in the Fanout cores, with $N_1:N_2 = 1:1$ for coupling through the register. The reason for suggesting, in Fig. 9, that 2, 10 is preferred--rather than 1, 5--is to make it easier to have the Fanout cores operate at a lower current level than the minor apertures. For the resistor coupling, the step-up ($N_5:N_6 = 1:5$) must be the same in this case as for the redundant switch. The primary advantage for the

second alternative is that somewhat less driver power is needed for the resistor connection than for driving the Fanout cores.

G. Register Voter Circuit

The Voter illustrated in Fig. 10 is a new circuit, but its operation has been verified in the laboratory except for one item: The

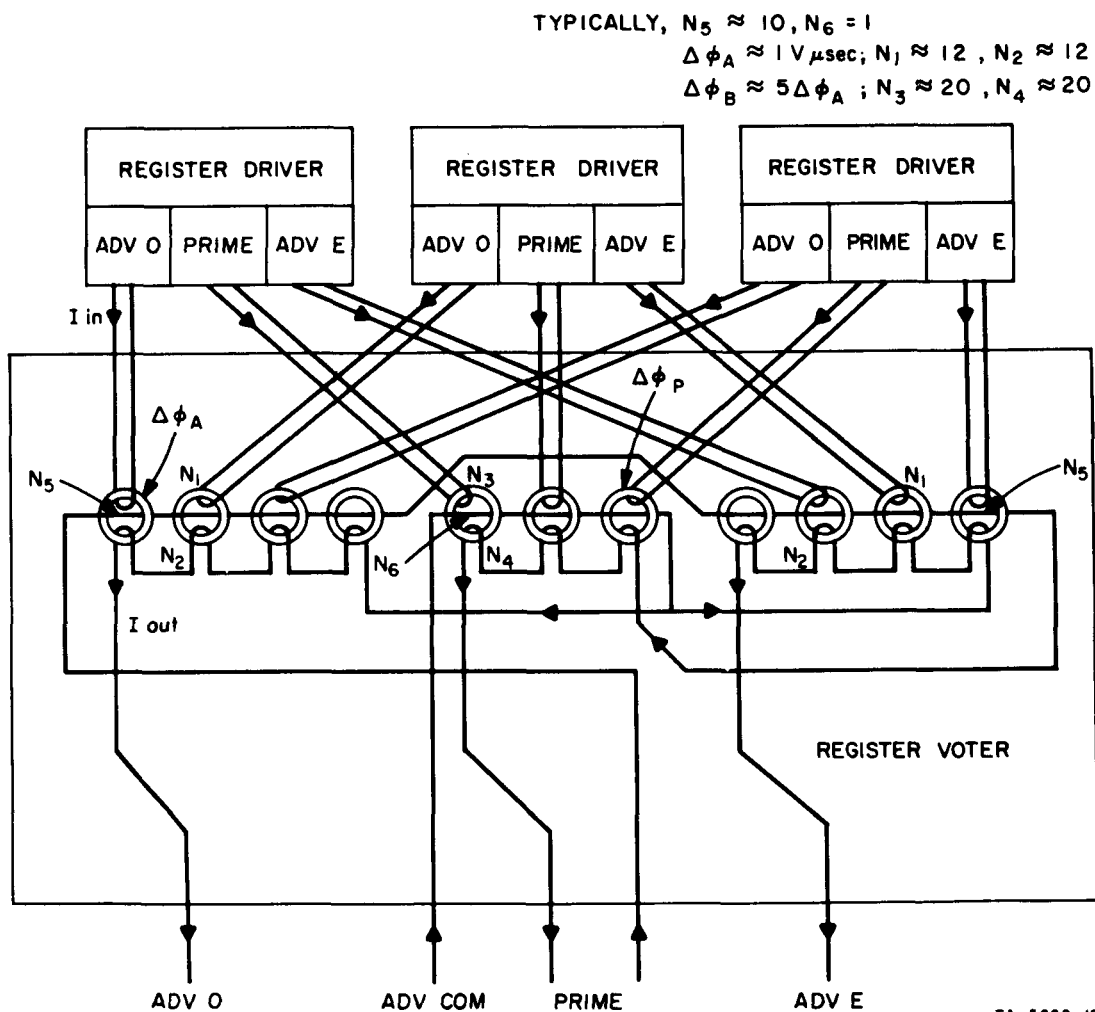


FIG. 10 SCHEMATIC OF REGISTER VOTER

Prime cores (center three) were reset with an external driver, rather than by Advance current as shown. It should be feasible to incorporate this latter feature, but there are two other alternatives. First, the

Prime cores could be linear material, provided the Prime current is designed to have a fall-time even greater than its rise-time. Second, the Prime Drivers could be designed to supply bipolar pulses.

1. Advance Voting

To understand how the Voter works, first note that one core in each Advance group:

- (1) Is not linked by an input winding
- (2) Is linked by the output winding in opposite polarity from the other three cores in the group.

Only a small positive current in the secondary loop is needed to exceed the threshold of this core and cause switching that bucks the switching due to any active combination of the other three cores. This current remains low (well below the threshold for transfer in the register) until the bucking core is fully switched.

In case only one other core in the set is switching (one of three Advance Drivers active), almost complete cancellation occurs, and the Advance current does not build up to an effective level. That is, the vote is for not shifting. If two cores are active, both switch about half way during the bucking period. Then Advance current builds up to an adequate transfer level as the two active cores switch the rest of the way, and the vote is for shifting. (It is of course taken for granted that in the detailed circuit design, the value of output flux linkage, $N_2 \Delta \Phi_A$, and the inherent impedances of the register Advance lines have been chosen to result in an Advance pulse of suitable width and shape.) If three Advance Drivers fire at once (normal operating conditions), the net secondary flux linkage is $2N_2 \Delta \Phi_A$ --double that for the previous case of two drivers firing. The circuit can be readily designed so that net switching mmf, $N_1 I_{in} - N_2 I_{out}$, is small compared to coupled mmf, $N_2 I_{out}$, in both cases. Hence, in the case of three, as compared with two drivers firing, the Advance pulse is only slightly higher but lasts twice as long or more, which does not significantly affect register operation.

2. Prime Coupling

It will be noted in Fig. 10 that only 3 cores are used for coupling Prime drivers into the output Prime circuit, and hence that voting against a single input, as described above for the Advance Drivers, does not take place. The reason this can be done is that prohibiting Prime current in case only one Register-Driver package is operating, is not necessary. For if only one Register-Driver package fires and flux is not transferred, Prime current has no effect on the register. A bucking core could be used to provide voting, but this would be a significant addition of ferrite and windings, since each Prime coupling core must provide about ten times the flux-linkage capacity of each Advance voting core. This is due to the fact that the Prime pulses must be very wide (about 200 microseconds as compared to a few microseconds for the Advance pulses).

The purpose of using core coupling for Prime is to isolate the Prime drivers from each other and provide some degree of current regulation to the register for the two cases of two or three Prime drivers firing. Assuming current drive for Prime, output amplitude remains quite uniform, with pulse width varying, as for the Advance drivers.

3. Drive-Line Impedances and Resetting Problems

Unlike the usual case of driving a MAD-R register, the Advance and Prime lines in this case are in fairly low-impedance circuits. Not only will spurious currents be induced in unused lines at the time of any one of the four pulses in the drive sequence, but also at any time when cores in the Voter circuitry are reset.

Fortunately, the resetting method indicated in Fig. 10 results in some cancellation of effects. Note that the Prime return links all Advance Voter cores in order to reset them at Prime time. The flux changes thereby coupled into Advance-current loops are of opposite polarity to that coupled in by the register, thus reducing the tendency for induction of spurious loop currents.

Some unbalance still occurs in general, and hence loop impedances must not be so low as to result in excessive loading of the register or in loop currents high enough to cause spurious switching of any cores. For registers required to store arbitrary patterns, the problems associated with low-impedance drive lines would be more serious. But here the pattern always contains only a single "1," resulting in a constant loading of the Voter, regardless of switch position. The initial laboratory experimentation has indicated that suitable impedances for the Advance lines may be obtained with normal wiring. It may be necessary to add extra inductance to the Prime line, but this could be readily achieved with a linear ferrite core linked by a winding in the output Prime loop and hence is consistent with the core-wire nature of the Voter.

In any case, some currents will be induced in all drive lines upon application of any pulse in the drive sequence, and this may call for some modification of relative numbers of drive turns from those indicated in Fig. 7 for the register.

H. Estimates of Driver Requirements, Performance, and Component Counts

1. Nominal Driver Requirements

Since the numbers of turns on register drive windings may be scaled uniformly, the volt-amperage requirements of the switch are in a sense more significant than voltage or current levels alone. Yet in general, this requirement is not entirely independent of the number of turns; for if drive line impedance is being minimized, the proportion required for the wire alone, versus the core contribution, decreases as turns increase. However, because of other requirements on drive-line impedance here (see previous section), we can assume constant volt-amperage to a first approximation, and hence all requirements are given relative to minimum numbers of turns. For scaling to a turns multiplying factor of n , one of course merely divides current and multiplies voltage by n .

When speaking of required current, we mean the peak value of a half cycle of a damped sinusoid, or of some other pulse with slow rise and fall compared to pulse width. The voltage value is also for the peak value, which does not necessarily occur at the same time as peak current. The one additional factor that must be considered is the voltage-time integral (flux-linkage capacity) needed to induce a drive pulse of adequate width in addition to the required amplitude.

The values given in Table I are for the redundant switch. The primary differences for the nonredundant version are as follows:

- (1) About 25% more volt-amperage from the Advance Drivers would be required in order to overcome losses in the Voter cores.
- (2) About 10% more volt-amperage would be needed for priming through the Prime-coupling cores.
- (3) The information drivers would have to supply about twice as much current and half as much voltage (assuming the fanout alternative using toroidal cores, rather than resistors).

Table I

NOMINAL DRIVER REQUIREMENTS FOR REDUNDANT COLLECTOR

Pulse	Preferred Pulse Shape	Approximate base width (sec)	Peak current (amps)	Peak voltage (volts)	Flux Linkage (volt- μ sec)	Turns Assumed
Advance	Damped Sine	10	5	20	15	$N_c = N_{xh} = 1$
Prime	Damped Sine or Triangle	200	0.5	1	100	$N_p, N_b = 2, 1$
Information Drive	Triangle	0.3	0.6	4	0.5	$N_1 = 1$
Information Reset	Triangle	0.6	0.4	20	2	1 turn/core

2. Estimates of Performance

Estimates of drive-pulse tolerances for the redundant switch are given in Table II. These estimates for the nonredundant switch would be comparable except for Prime current.

Table II

ESTIMATE OF COLLECTOR DRIVE TOLERANCES

Pulse	Nom. Value (amp)	Tolerances at Room Temp. (%)		Temp. Tolerance for Fixed Drive, No Heating (°C)		Tolerance for Range of -10°C to +85°C, with Possible 10°C Internal Rise (%)	
		Lower	Upper	Lower	Upper	Lower	Upper
Advance	5	-20	+500	-50	100	-10	+100
Prime	0.5	-30	+200	-40	100	-10	+ 10
Information Drive	0.6	-30	+100	-20	100	-10	+ 10
Information Reset	0.4	-30	+100	-20	100	-10	+ 10

3. Estimate of Dimensions

The register cores are about 0.4 inch in diameter. Assuming cores on edge, and O and E cores in side-by-side lines, one register would take up a space about 1/2 inch x 1 inch x 4 inches or 2 cubic inches. The Register Voter would require about an equal volume, and the Fanout cores about 1 cubic inch more. Thus the redundant switch with three registers would require about 6 cubic inches, whereas the nonredundant one with Voter and Fanout circuits would need about 5 cubic inches of volume.

4. Component Counts

In Table III, component counts are estimated for both switches, since this is a potential factor for choice of one or the other. Note that the main differences are more MADs (with more turns per minor

Table III

ESTIMATE OF COMPONENT COUNT FOR CYCLIC COLLECTOR

Component	Number of Components	
	Redundant Switch	Nonredundant Switch
Multiaperture Cores (MADs)	72 (Note 1)	24 (Note 1)
Toroidal Cores	0	41 (Note 2)
Solder joints:		
coupling loops	18	6
prime loop	0	6
advance loops	2	6
information drive	6	6
information output	0	6
Total solder joints	26	30
Interface Terminals	≈ 80-100	≈ 80-100 (Note 3)
Length of Wire	25 (Note 4)	25 (Note 4)
Turns (Note 5):		
Max. in minors	7	5
Aver. in minors	6	3
Total in minors	≈ 400	≈ 100
In each major	2	2
Total in majors	36	12
Max. in toroids	0	41
Aver. in toroids	0	20
Total in toroids	0	≈ 600
Total turns	≈ 440	≈ 710

Notes:

1. Assuming 6 for each O stage and 2 for each E stage
2. Assuming stacks of 5 for each Prime-coupling core
3. Depending on single- or double-wire lines from Information Drivers
4. More information wiring for redundant switch, versus extra wiring required for the Voter in the nonredundant case.
5. Assuming minimum turns for register drive windings.

aperture) for the redundant switch versus inclusion of toriods with many-turn windings for the nonredundant switch.

I. Potential Improvements

The alternatives discussed above for the Cyclic Collector Switch are based on techniques that are well known, or laboratory tested on this project, and on proven core designs. Some circuit and core refinements can be thought of that could ultimately lower the drive requirements of this type of switch by a moderate factor. Development of sound new core designs to the production stage seems to be a fairly long-term process, so it is assumed that a first prototype model of the switch would use present cores. However, circuit refinements could be incorporated in such a model if first proven sound in the laboratory.

1. Possible Circuit Improvements

Note that one bit-length of the register (Fig. 7) includes two stages (one O and one E). This register design is inefficient in the sense that only the Odd cores are used for coupling information, whereas the Even cores stand idle except during the shifting of switch position. By applying only one-half of a full clock cycle for each advancement of switch position, we could use E as well as O stages for positions and hence have half the number of register bits in general. For the present case of three positions, $1\frac{1}{2}$ bits would be implied, but this is impossible for a closed-loop register, so it would be necessary to use 2 bits, a reduction of only $\frac{1}{3}$ from the case of one bit per position. The price paid would be some additional logic (redundant) at the interface going from Hard Control to the Register Drivers, in order that these drivers provide alternate half cycles of drive in response to signals to advance.

An alternate way to reduce the number of register cores by 50% is to leave both the O and E stages of the active bit-length set at the end of a clock cycle. This can be done by means of nondestructive transfer from E to O (i.e., leaving the prior E stage as well as the new O stage in a set state). Then each register stage would consist

of only three thin cores in order for six bits of information to be handled. The price paid here is that one extra driver (triplicated), along with an extra cell in the Voter, would be needed to clear the E cores as a first step, prior to the Adv O drive, upon receipt of the next advance signal from Hard Control.

2. Core Improvements

Design of a smaller core adapted to this application could reduce the register drive current requirements approximately by a factor of two, and the information drive by about 30%. Use of a slightly lower-threshold material, but one still having good temperature stability, might reduce both by another factor of 30%. Thus both of these improvements used in conjunction could reduce register drive by about two-thirds and information drive by one-half.

3. Conclusion

The conceivable circuit and core improvements together might reduce register volt-amperage requirements to 25% of those estimated here and information drive by 50%.

IV SELECTOR COLLECTOR

A. Introduction

This Selector Collector switch differs from the Cyclic Collector switch in that signals from the Hard Control indicate which Arithmetic Unit is to be connected, rather than that the next one in line is to be taken.

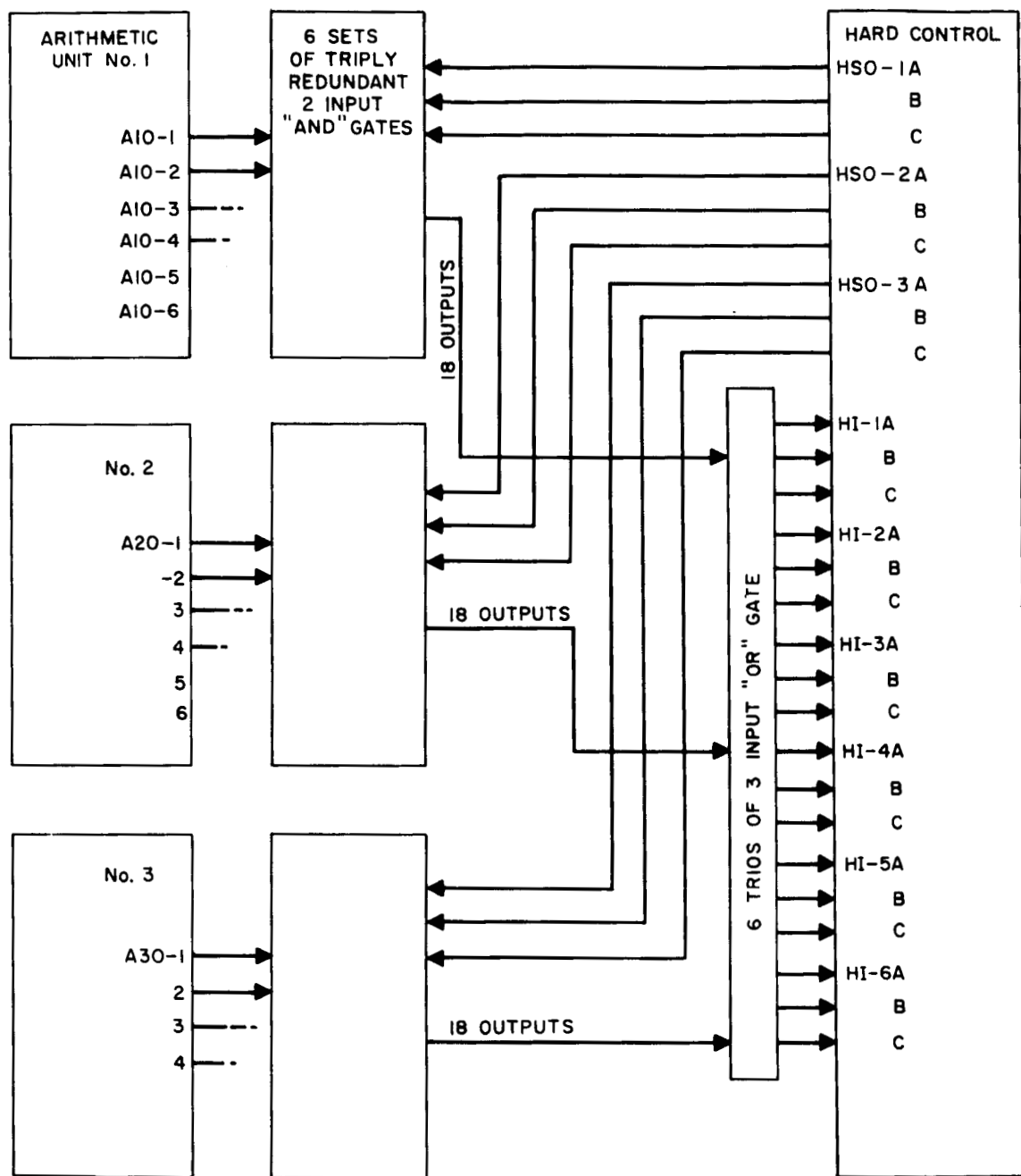
Since there are only three redundant copies of subsystems to choose from, coding the signals does not reduce significantly the amount of hardware required. The switch described here will assume a separate triply redundant output line from the Hard Control for selecting each Arithmetic Unit.

The Selector type switch puts on the Hard Control the burden of remembering the switch position through power failure and during normal operation.

One version of this switch will be described in detail and two others only briefly.

B. Redundant Selector

The block diagrams of the redundant toroid version of the switch are shown in Figs. 11 and 12. The switch is essentially a fan-out from the nonredundant channels of the Arithmetic units to the three channel redundant AND gates. These gates are followed by three input OR gates to provide the fan-in from three arithmetic units to one control unit. Triple redundancy is maintained in the magnetic circuitry as well as in the drivers. A partial schematic diagram is shown in Fig. 13. Each nonredundant Arithmetic Unit output is connected to each triply redundant Hard Control input through a triply redundant AND gate. The three cores connected to each Arithmetic Unit output shown in Fig. 13 are an example of this triply redundant AND gate. The output of the Arithmetic Unit is connected through a driver to the three set windings in series. When the three cores switch, voltages are induced



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FIG. 11 SIMPLIFIED BLOCK DIAGRAM OF REDUNDANT SELECTOR

in the three output windings that drive the three redundant inputs to the first information input channel of the Hard Control. Since this information channel must receive signals from all of the Arithmetic Units, the output windings of the corresponding gate cores are connected to it in series.

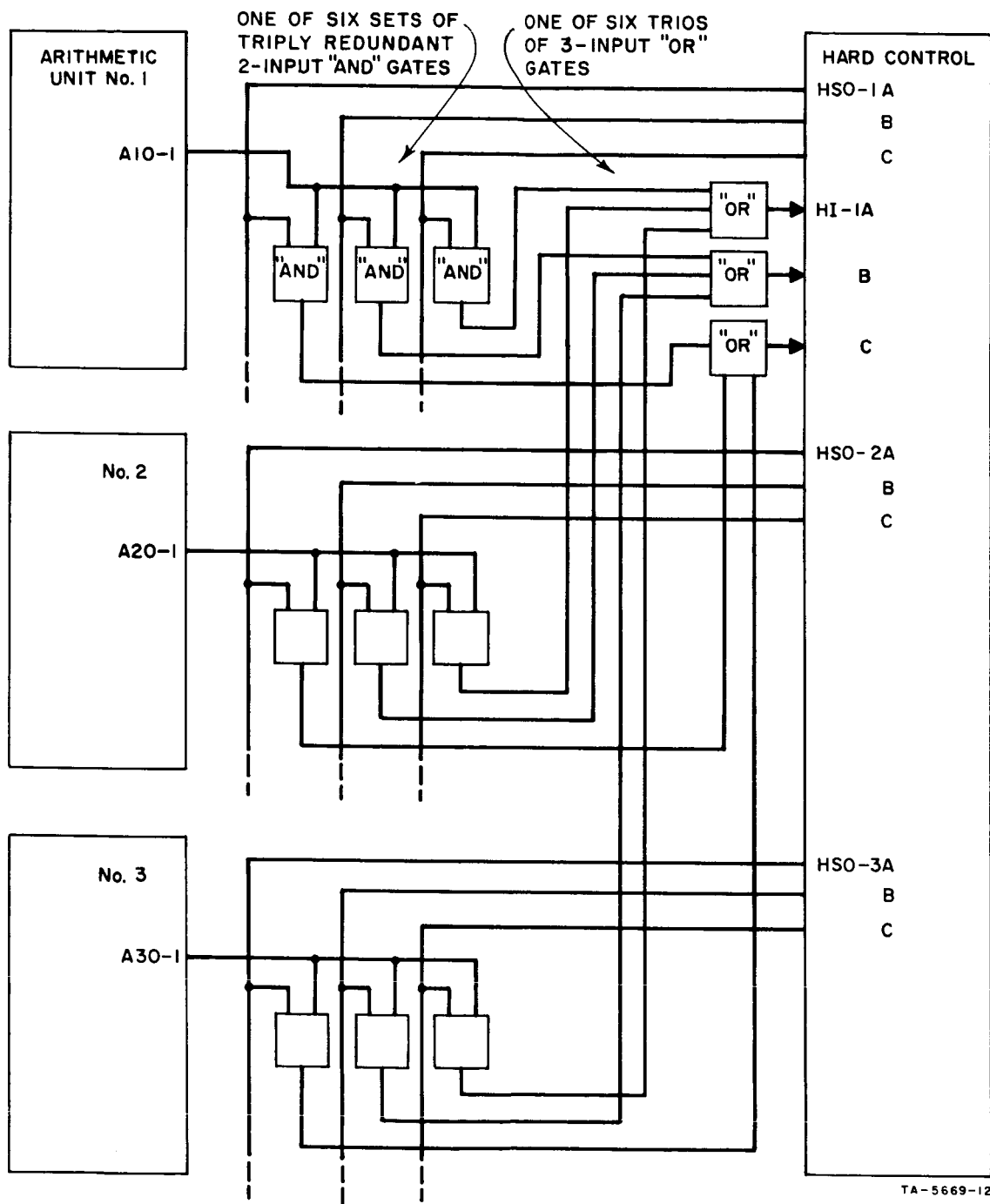


FIG. 12 DETAILED PARTIAL BLOCK DIAGRAM OF REDUNDANT SELECTOR

No signals will appear on the output windings unless the cores are reset each clock cycle. It is through this reset operation that the desired Arithmetic Unit is selected. The Hard Control sends reset pulses

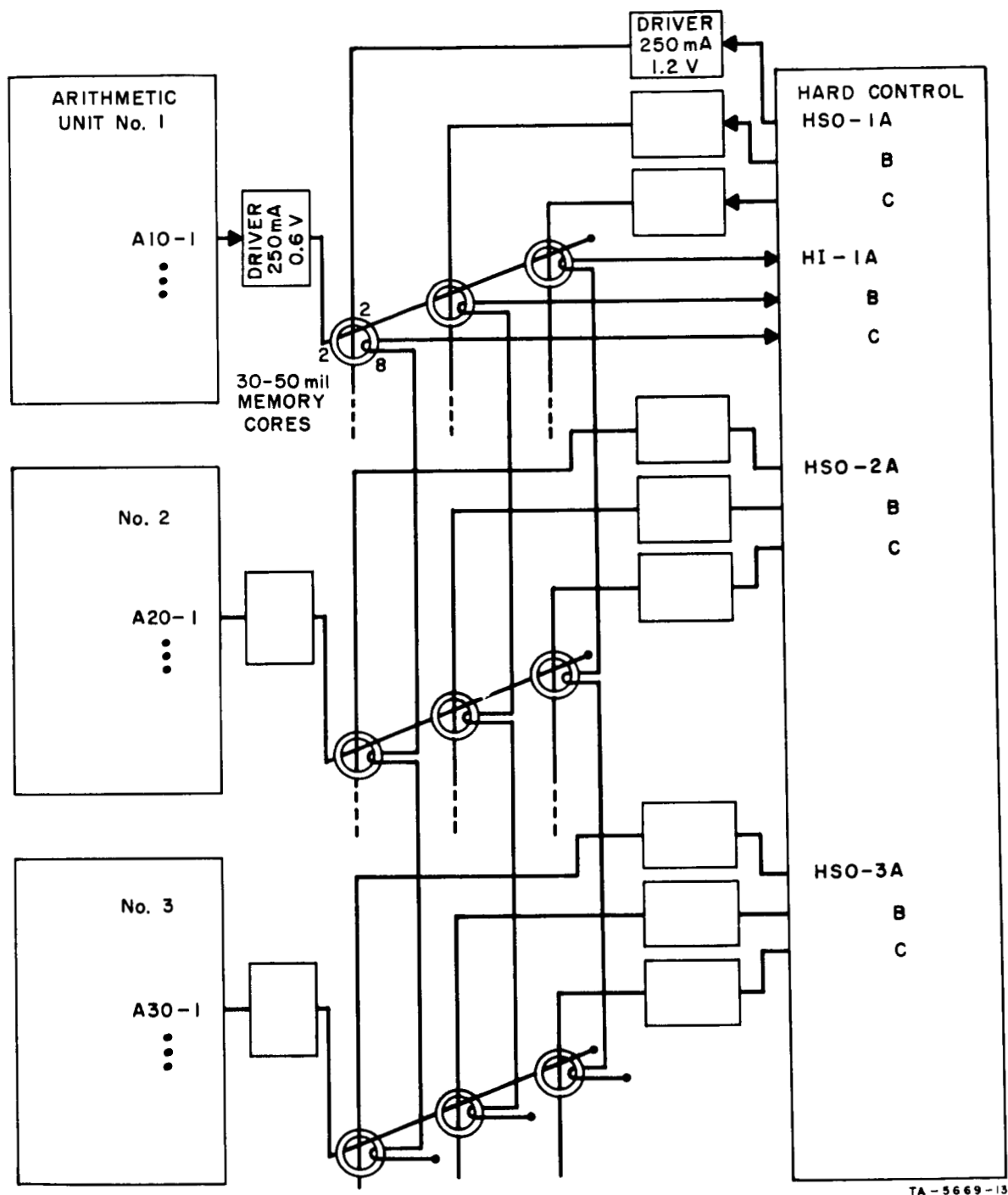


FIG. 13 SCHEMATIC DIAGRAM FOR REDUNDANT SELECTOR

to the cores corresponding to the Arithmetic Unit that is selected. Each one of the three redundant selection outputs provides the pulse to reset one out of each set of three gate cores, thus maintaining the three independent channels. If any one channel fails, the next voting circuit inside the Hard Control corrects the error.

A driver is required on each output of the Arithmetic Units and each selector output of the Hard Control. The primary design consideration in this version of the switch is a good compromise between core cross section and number of turns in obtaining sufficient voltage to drive the MECL circuits in the Hard Control. A 50-mil-ID, 80-mil-OD memory core provides a reasonable compromise. The required 12 turns is practical for this size core. Two turns were chosen for the set and clear windings as a reasonable compromise between current amplitude required from the driver and numbers of turns to wind on the core.

C. Nonredundant Selector

The block diagram of the Nonredundant Selector is shown in the block diagrams of Figs. 14 and 15. In this version the gate cores are not triply redundant. The selector signals from the Hard Control feed into a voting circuit, the output of which controls the gates for the Arithmetic Unit signals. The output of these gates goes to an OR gate, after which fanout to the triply redundant channels of the Hard Control is accomplished.

The circuit diagram of Fig. 16 shows the voting circuit for the redundant selection outputs of the Hard Control. This voting circuit is the same type as that used in the Cyclic Collector, but the inhibit type voter used in the Distributor is also applicable here.

The gate core operates in the same way as in the preceding version except that the fanout is made with three separate output windings from the same core. Three windings were used instead of one, so that either an open or shorted winding could be tolerated on any gate core without disabling the whole computer, and, in addition, the three channels of the Hard Control are isolated from each other.

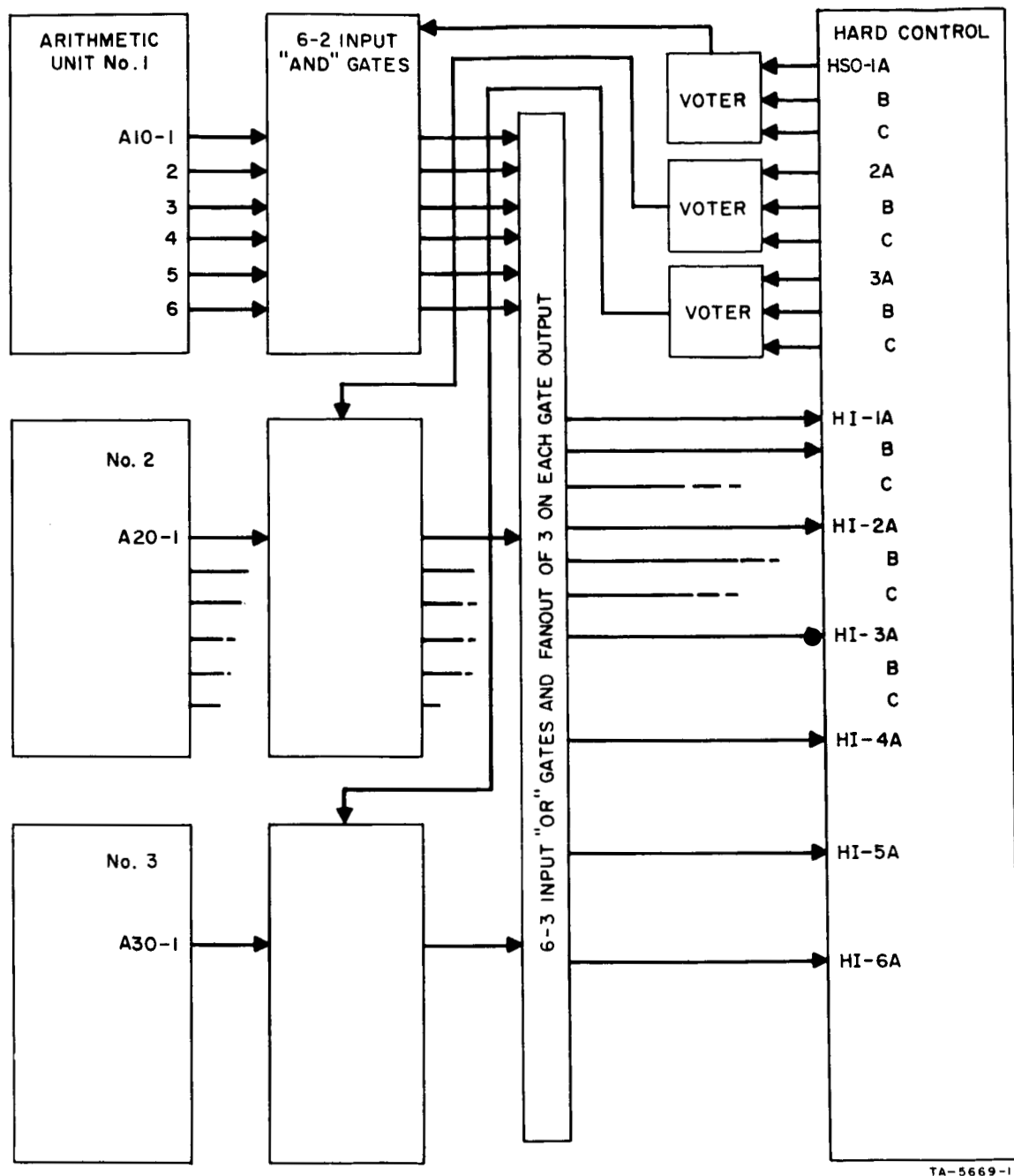


FIG. 14 SIMPLIFIED BLOCK DIAGRAM OF NONREDUNDANT SELECTOR

The voting cores are cleared while the Arithmetic Unit pulses are setting the gate cores. This clearing will have to be done at a low enough switching rate to prevent setting of any gate cores with the induced coupling loop current. Letting the coupling loop set the cores

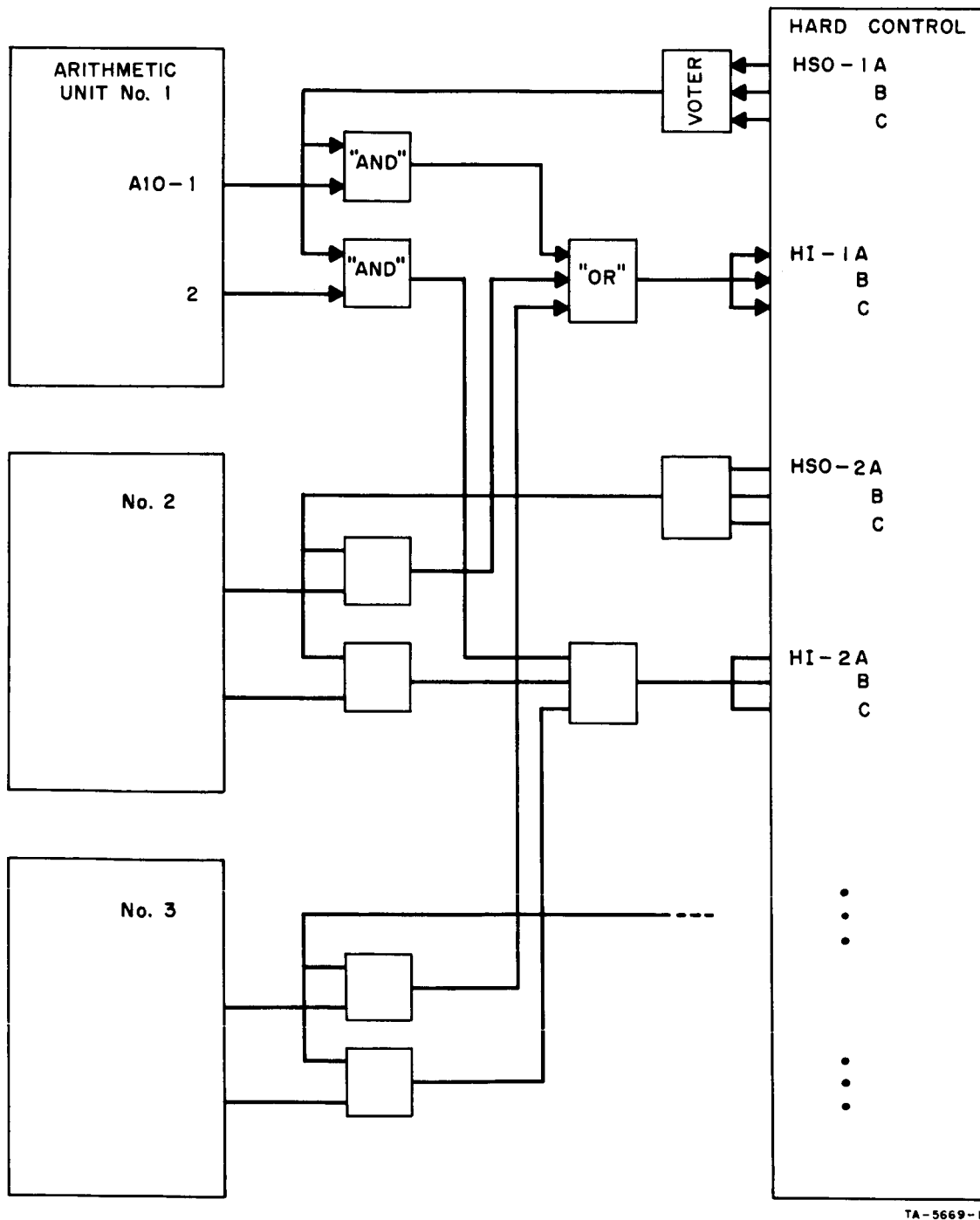


FIG. 15 PARTIAL BLOCK DIAGRAM OF NONREDUNDANT SELECTOR

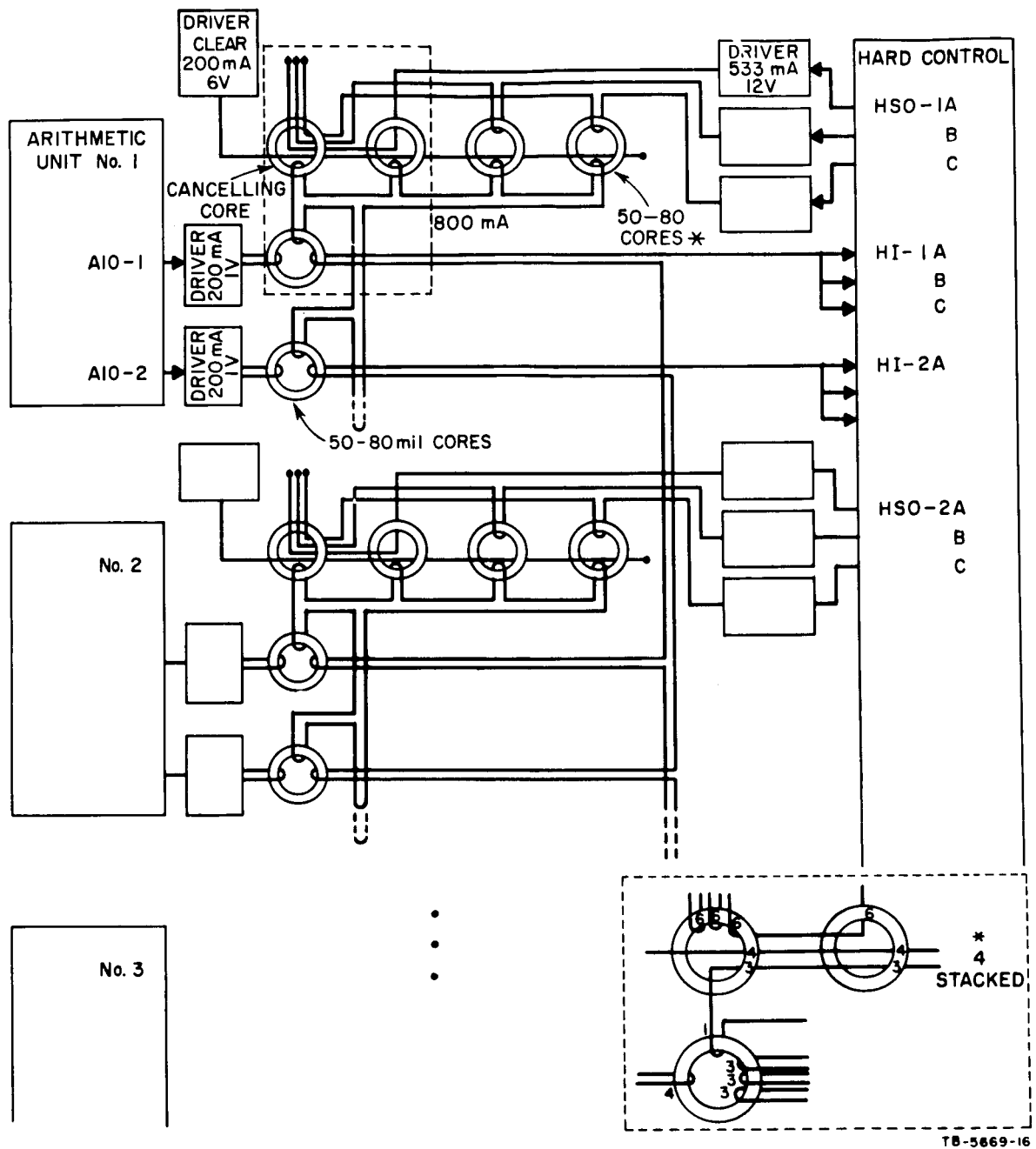


FIG. 16 PARTIAL SCHEMATIC DIAGRAM OF NONREDUNDANT SELECTOR

and the information drivers inhibit them is a solution to the clearing problem. This approach was suggested by George Hansen of JPL.

Larger cores (50-mil ID, 80-mil OD) are required for this circuit than in the preceding one, both in the voter circuit and gating circuit,

because in both cases more windings are required. The cancelling core in the voter circuit has three set windings because all set windings for the other cores in the voter circuit must link the cancelling core. The voter cores are made thicker by stacking four cores of the size used in the gates. This larger cross section is required to obtain sufficient flux capacity for driving the gate cores without using an excessive number of turns. This many turns is not excessive for the 30-50-mil core but if it were used, 2-1/2 times as many turns would be needed on the output windings because the voltage per turn is smaller. This would make a total number of turns of about 25, which would be excessive.

Another version of this switch eliminates the voter circuit by having the clear drivers connected in parallel to a single select winding as shown in Fig. 17. Any short in a select winding or driver would have the same effect as a failure in the associated Arithmetic Unit. Two out of three of the drivers could fail in any mode where their output impedances were maintained at a sufficiently high value.

Each driver could be connected to a separate select winding but probably the reliability would be decreased more by the added windings than increased by the added capability of tolerating an open circuit in two out of the three select windings.

D. Comparison of Selector Type Collectors

The comparison between the first version, which is triply redundant throughout, with the second, which has nonredundant gates, shows some surprising results. The advantages that might be expected in going to a nonredundant circuit are not realized in practice because of some of the basic characteristics of the voting circuits. The comparison will be made between the first two versions on the basis of reliability, power, cost, and volume. The last version will be discussed separately. The following arguments are based on the estimates shown in Tables IV and V.

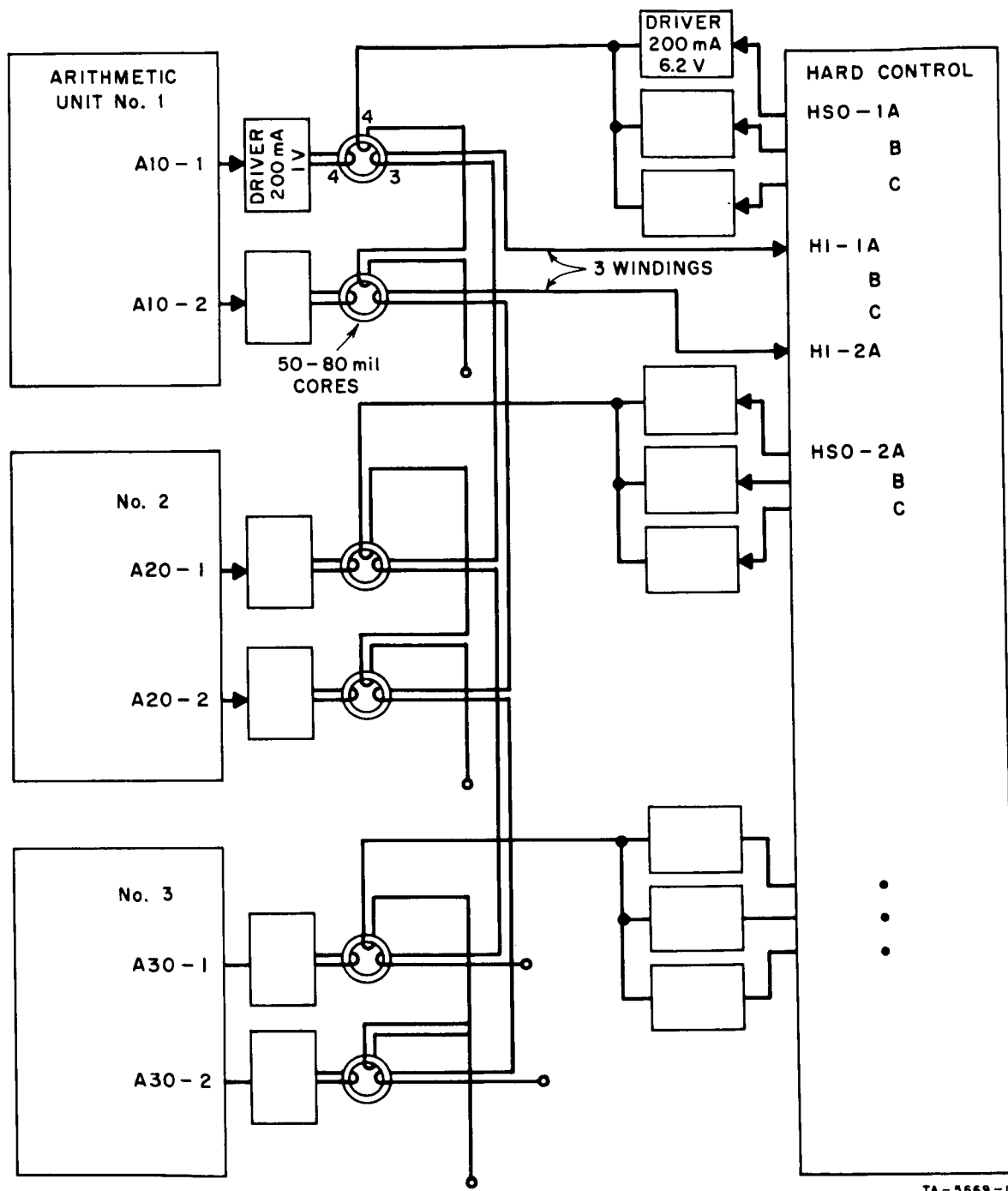


FIG. 17 NO-VOTER VERSION OF NONREDUNDANT SELECTOR

Table IV

DRIVER REQUIREMENTS FOR SELECTOR COLLECTOR

	Redundant Selector	Nonredundant Selector
Information Driver Requirements		
Voltage	.6	1.0
Current (amps)	.25	.20
Selection or Voter Driver Requirements		
Voltage	1.2	12.6
Current (amps)	.25	.533
Voter Clear Driver	none	
Voltage	-	8
Current (amps)	-	.350
Total Peak Power for Selector (watts)	2	7.6
Total Average Power for Selector (watts)	1	3.8

Note: Clock rate = 1 Megacycle

Temperature range = -10°C to +85°C

Power relates to the cores; driver power is not included here

1. Reliability

Reliability depends upon the number of drivers, their redundancy arrangement, total number of turns wound on cores, turn density, redundancy of magnetic circuits, and number of solder joints.

The first version is better, relative to all the above considerations except number of turns and turn density. The advantage of the second version here is slight because the number of turns is only 30% less, and the voter cores are complicated by the fact that the cores are stacked four deep and the cancelling core has 25 turns on it. The number of solder joints is not as significant as the fact that most of them are included in the redundancy in the first version, but not in the second. The first version is thus more reliable from the overall point of view.

Table V

ESTIMATE OF COMPONENT COUNT FOR SELECTOR COLLECTOR

	Redundant Selector	Nonredundant Selector
Core size (mils)	30-50	50-80
Total number of cores	54	30
Maximum turns per core	12	25
Average turns per core	12	15
Total turns for the Selector	648	450
Total number of solder joints (not including drivers)	90	96
Total number of drivers	27	30

2. Power

Even though there are more cores in the first version, it requires less than 1/3 the power because the cores are so much smaller. This stems predominantly from the fact that each voter output winding must have a flux linkage capacity equal to the sum of all six gate-core reset windings. Considering practical configurations of core geometry and number of turns, the result is that the increase in volume of ferrite in the voter circuit more than compensates for the decrease in volume of ferrite due to the reduction in the number of gate cores. The efficiency of the drivers was not considered in the above argument. The drivers are treated in a separate section.

3. Cost

The total cost depends mainly on the cost of fabrication. The difference in cost of fabrication of these two versions is difficult to estimate and is probably not very significant since there are compensating factors involved such as the fact that the cores are smaller in the first version but the second version has cores stacked four deep.

4. Volume

The volume depends mainly on the drivers. The first version has a slight advantage here in that it has a few less drivers (no clear drivers) and they generally have to switch less power.

The third alternative for the Selector-Type Collector was expected to be superior to the other two in all respects except for a significantly lower level of reliability. The requirement for triple output windings, however, prevented it from being significantly superior to the first version. The triple output windings required a larger core which in turn increased the power. This alternative did not turn out to be competitive with the other two.

The comparison between the Cyclic Collector Switch and the Selector Collector Switch is a matter of weighing the advantage of the lower cost of the Selector Switch against the disadvantage of increasing the complication of the Hard Control by making it remember the switch position and select a particular subsystem rather than the next one in line. The cost saving tends to be less significant than might be expected because the number of drivers required is the same for both switches. The saving stems mainly from the use of toroids rather than multiaperture devices and from less complicated wiring and driver sequencing. The main feature that makes the Cyclic-Type Collector the better choice is that it maintains its position during power failure without complicating the Hard Control.

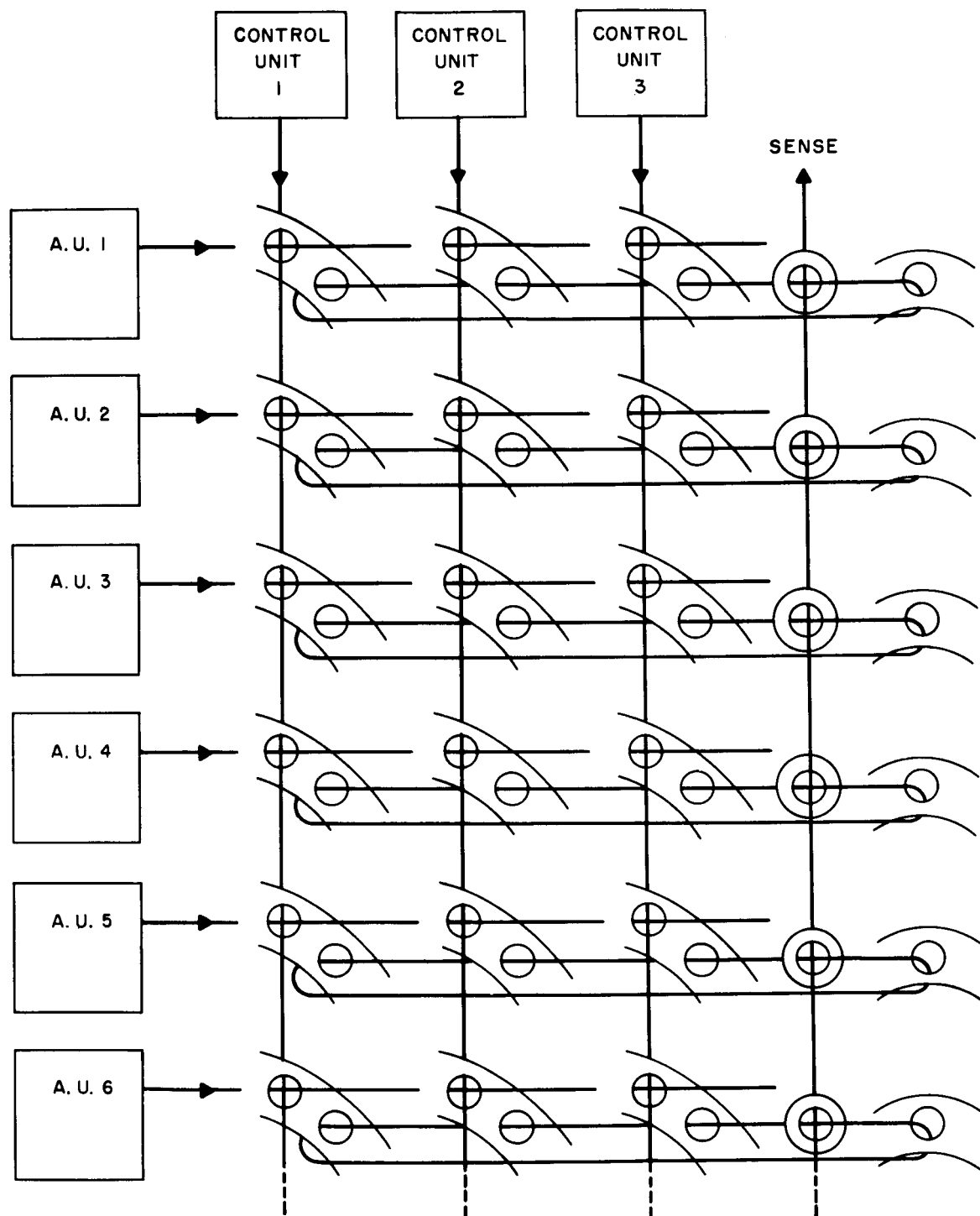
Estimates of performance and component counts are given in Tables IV and V.

V N-OUT-OF-M SELECTOR SWITCH

The N-out-of-M Selector Switch is of interest only for later development of the switch beyond its present capability. A circuit approach to this switch is described briefly here for future reference.

The problem and the approach to a solution are similar to the Cyclic Collector in that a shift register is used to select a particular arithmetic unit. The basic difference is that the shift register must shift some varying number of times, rather than just once, to select the next spare arithmetic unit. A partial circuit diagram of the switch is shown in Fig. 18. Three arithmetic units are working simultaneously, each one connected to its corresponding control unit as indicated in the figure. The apertures of the set cores are unblocked, connecting Arithmetic Unit 1 to Control Unit 1, Arithmetic Unit 2 to Control Unit 2, etc. Assume that Arithmetic Unit 2 fails. Shift Register 2, corresponding to Control Unit 2, must be shifted two stages to provide a connection to the next spare arithmetic unit which in this case is number 4. Register 2 is shifted until the position of its set state corresponds to that in the Selection Shift Register. The purpose of the Selection Shift Register is to indicate the position of the next available spare arithmetic unit. The detection of coincidence between the two registers is accomplished with a toroid sense core on a coupling loop between the registers, as shown in the figure. When the minor apertures of corresponding cores switch, their induced voltages in the coupling loop cancel and the sense core does not switch. When they do not coincide, the sense core switches, inducing a voltage in the sense coincidence line indicating that another shift is required.

Switch control circuitry is needed which sends shift pulses to the Selection Register and the appropriate Connection Register when signals are received on the sense coincidence line. Circuitry is also needed to provide the drive pulses for coincidence sensing.



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FIG. 18 N-OUT-OF-M SELECTOR

VI DISTRIBUTOR

A. Introduction

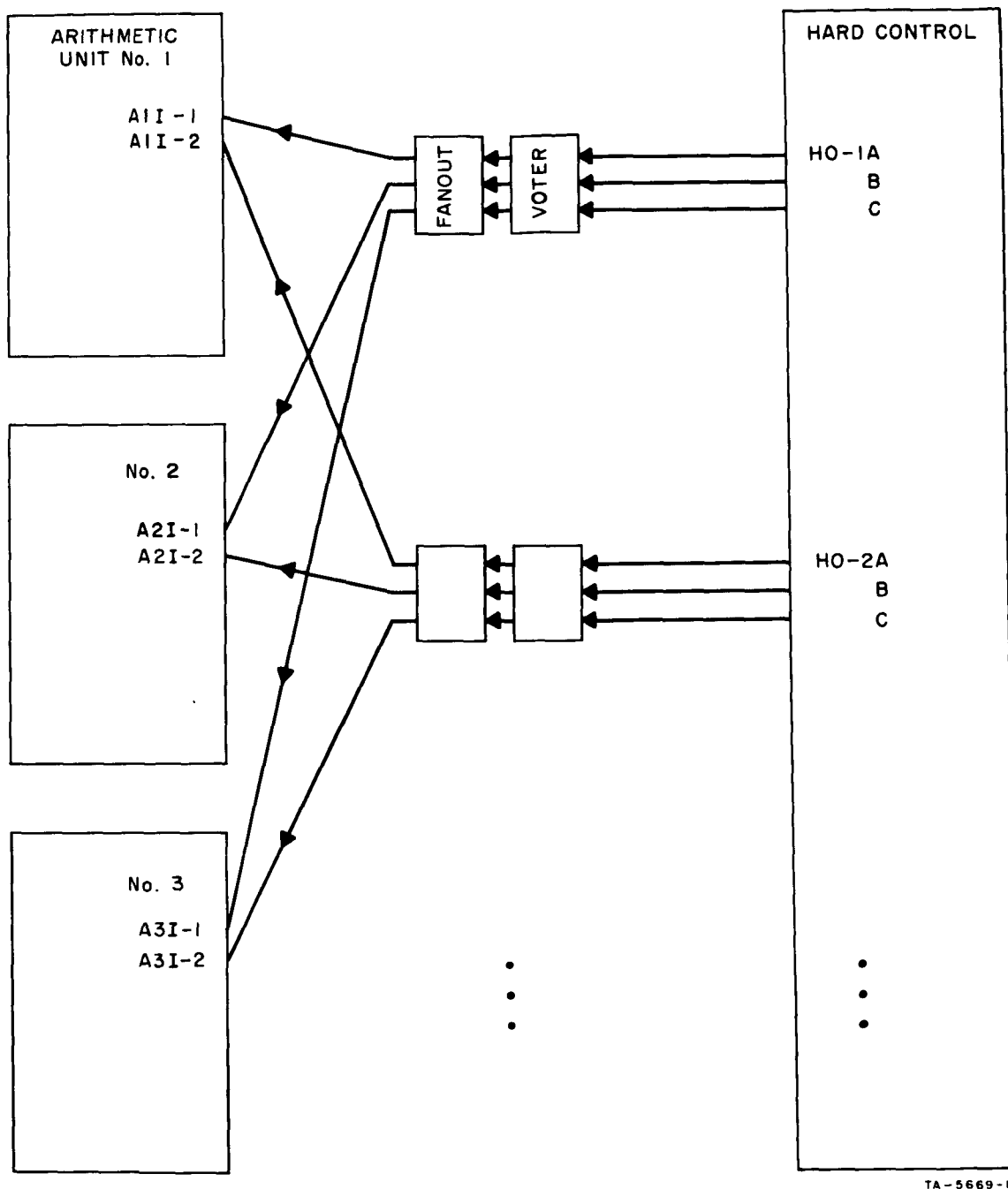
In the Distributor, information flows from the Hard Control to the Arithmetic Units. The operation involved here is accomplished by fanning out to the three Arithmetic Units (rather than by switching) as shown in Fig. 3. It is assumed that no undesirable result can occur due to signals on the inputs to Arithmetic Units, which are not being used whether or not they have power applied. A voting circuit is needed either before or after fanout, to combine the three redundant outputs from the Hard Control for each of the four bits in an information channel.

Three alternative circuits for the switch will be described. They will be compared with each other in terms of numbers of components, driver requirements, power requirements, and performance.

B. Single-Voter Distributor

The Partial Block Diagram for the Single-Voter Distributor is shown in Fig. 19. A driver is connected to each of the three redundant outputs of each bit channel. The outputs of these are combined in one voter. The output of the voter fans out to the three copies of the Arithmetic Unit.

The schematic diagram of one voter and its associated fanout circuitry is shown in Fig. 20. The four square-loop cores and their associated windings connected to the drivers are the voting circuit. The three linear cores and their associated windings are isolating fan-out transformers. The voting circuit is the same type as that used in the Cyclic Collector Switch of Sec. III-G except that the load on this circuit is much easier to drive, but must operate at the high information pulse rate rather than the very low switching rate required for the changing of the position of the Cyclic Collector Switch. The voting circuit responds to three output modes of the Hard Control in the following way:



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FIG. 19 PARTIAL BLOCK DIAGRAM OF SINGLE-VOTER DISTRIBUTOR

- (1) When all three of the redundant outputs of the Hard Control put out a pulse, all four of the square loop cores (A thru D) switch. The cores are linked by the interloop in such a way that the voltage generated by

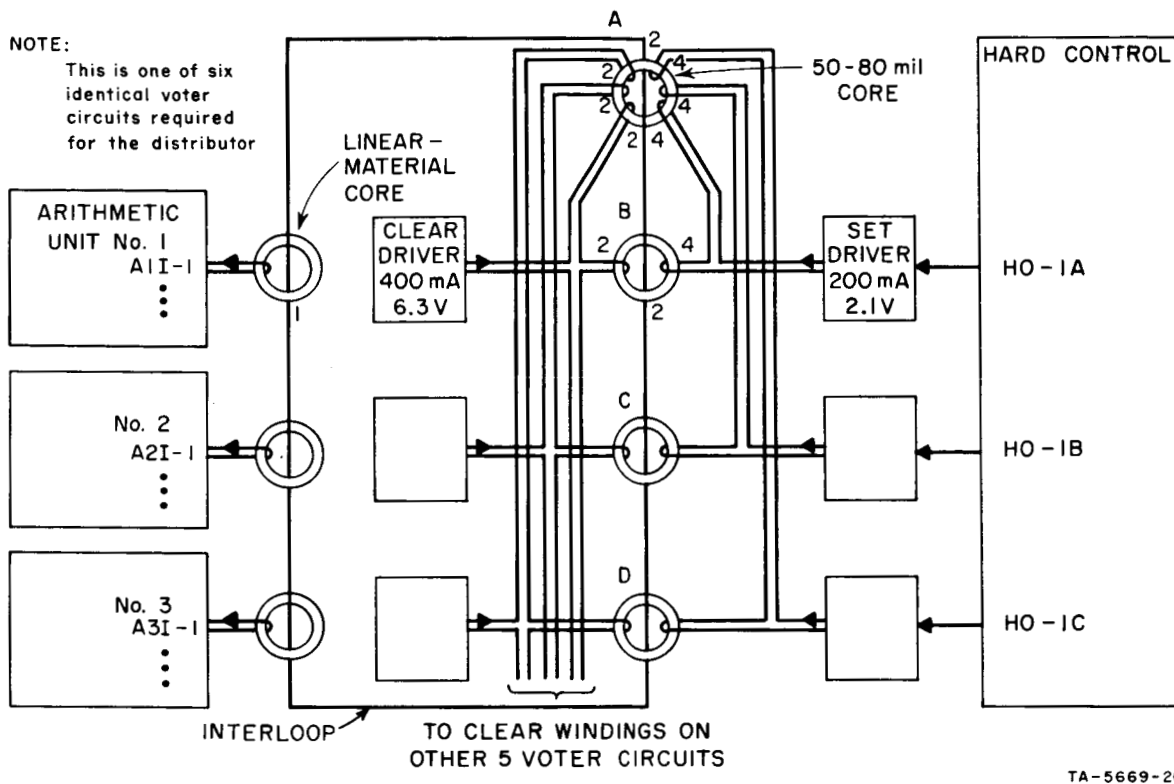


FIG. 20 SCHEMATIC DIAGRAM OF SINGLE-VOTER DISTRIBUTOR

the switching of Core A bucks that generated by the other three. Since Core A is driven by all three drivers, it switches almost three times as fast as each of the others and thus almost bucks out the voltage induced by the other three on the interloop. After Core A saturates, the other three cores, having $\frac{2}{3}$ of their flux left, continue switching, providing the voltage in the interloop to drive the Arithmetic Units.

- (2) If only one of the three redundant outputs of the Hard Control puts out a pulse, it is assumed to be erroneous. Assuming such a pulse input to Core B, Core B and Core A will both be driven by one driver and will switch at the same speed, inducing equal and opposite voltages on the interloop. Thus the

erroneous signal is not received by the Arithmetic Units.

- (3) If one of the three outputs of the Hard Control fails to put out a pulse, then the net effect is that the cancelling core cancels the effect of the remaining two cores during the first half of their switching. The last half of their switching induces a voltage in the interloop, which drives the Arithmetic Units.

Voltages induced in the interloop are coupled through the transformers into the Arithmetic Units. The input currents to the Arithmetic Units are small compared to the magnetizing currents of the transformers and thus the voltage induced in the interloop by the voter cores will distribute approximately evenly between the three transformers. The primary purpose of the transformers is to isolate failures in the Arithmetic Units since fanout could be achieved with parallel interloops.

The voter cores are cleared on the opposite phase of the machine clock. Two alternative ways of clearing are available:

- (1) The set drivers could provide bipolar outputs such that a reverse polarity clear pulse followed each normal pulse on the same output line.
- (2) Separate clear drivers can be used. Three clear drivers are needed to provide the clear pulses for all six voters. Each clear pulse driver drives the six cores that correspond to a particular one of the three redundant Hard Control channels of all six outputs, as indicated in Fig. 20.

The three separate clear drivers will probably require fewer components than the additional number that would be required to make the eighteen set drivers bipolar.

Voltage induced on the interloop during the clearing of the voter cores is of the wrong polarity to cause any switching in the Arithmetic Units.

The mmf induced by the interloop current on the voter cores is small compared to their switching mmfs and will, therefore, have negligible effect upon their switching rates. The tendency is for this current to make the cancelling core switch faster and the other ones slower. This will have no adverse effect upon the circuit operation.

The timing of the pulses from the drivers is not crucial because when cancelling is necessary the cancelling core is driven by the same driver as the core whose induced voltage must be cancelled.

The basic design problem here is to provide the necessary volt-microsecond signal at the Arithmetic Unit inputs with an appropriate compromise between low power and expensive fabrication. Low power is achieved by putting many turns on small-cross-section cores while economical fabrication (and to some extent increased reliability) is achieved by large cores with few turns. The ultimate goal in low power would be cores that could be driven directly from MECL NOR circuits. With present-day square-loop materials, this goal cannot be reached. The necessary core would have too large a diameter, too small a cross section, and require too many turns to be practical.

The detailed design will be worked out in the next phase of the project. The best estimates of core size, number of turns, driver requirements, etc. are shown in Fig. 20 and in Tables VI and VII.

C. Multiple-Voter Distributor

The Multiple-Voter Distributor has one voting circuit for each Arithmetic Unit input, as shown in the block diagram of Fig. 21. The drivers are shown on the Hard Control side of the fanout, but to obtain increased reliability at greater expense, a second alternative could be chosen where one driver is placed at each input to each voter, as shown in Fig. 22. This would require three times the number of drivers, but each one would have only one-third as much load.

The circuit for the voter is shown in Fig. 23. This is the same circuit as for the Single-Voter Distributor except that no isolating fanout transformers are needed in this case, and the drivers drive three

Table VI

DRIVER REQUIREMENTS FOR DISTRIBUTOR

	Multiple- Voter Distributor	Single- Voter Distributor	Multiple- Inhibit-Voter Distributor
Information Driver Requirements			
Voltage	6.3	2.1	1.2
Current (amps)	.200	.200	.250
Clear Driver Requirements			None
Voltage	10	6.3	-
Current (amps)	.8	.40	-
Total Peak Power for Distributor (watts)	8.3	2.8	2.0
Total Average Power for Distributor (watts)	4.2	1.4	1.0

Note: Clock rate = 1 Megacycle

Temperature range = -10°C to +85°C

Power relates to the cores; driver power is not included here.

Table VII

ESTIMATE OF COMPONENT COUNT FOR DISTRIBUTOR

	Multiple- Voter Distributor	Single- Voter Distributor	Multiple- Inhibit-Voter Distributor
Core Size (mils)	50-80	50-80	30-50
Total number of cores	72	42	54
Maximum turns per core	21	20	12
Average turns per core	12	7.5	12
Total turns for the Distributor	864	315	648
Total number of solder joints (not including drivers)	78	79	84
Total number of drivers	21	21	24

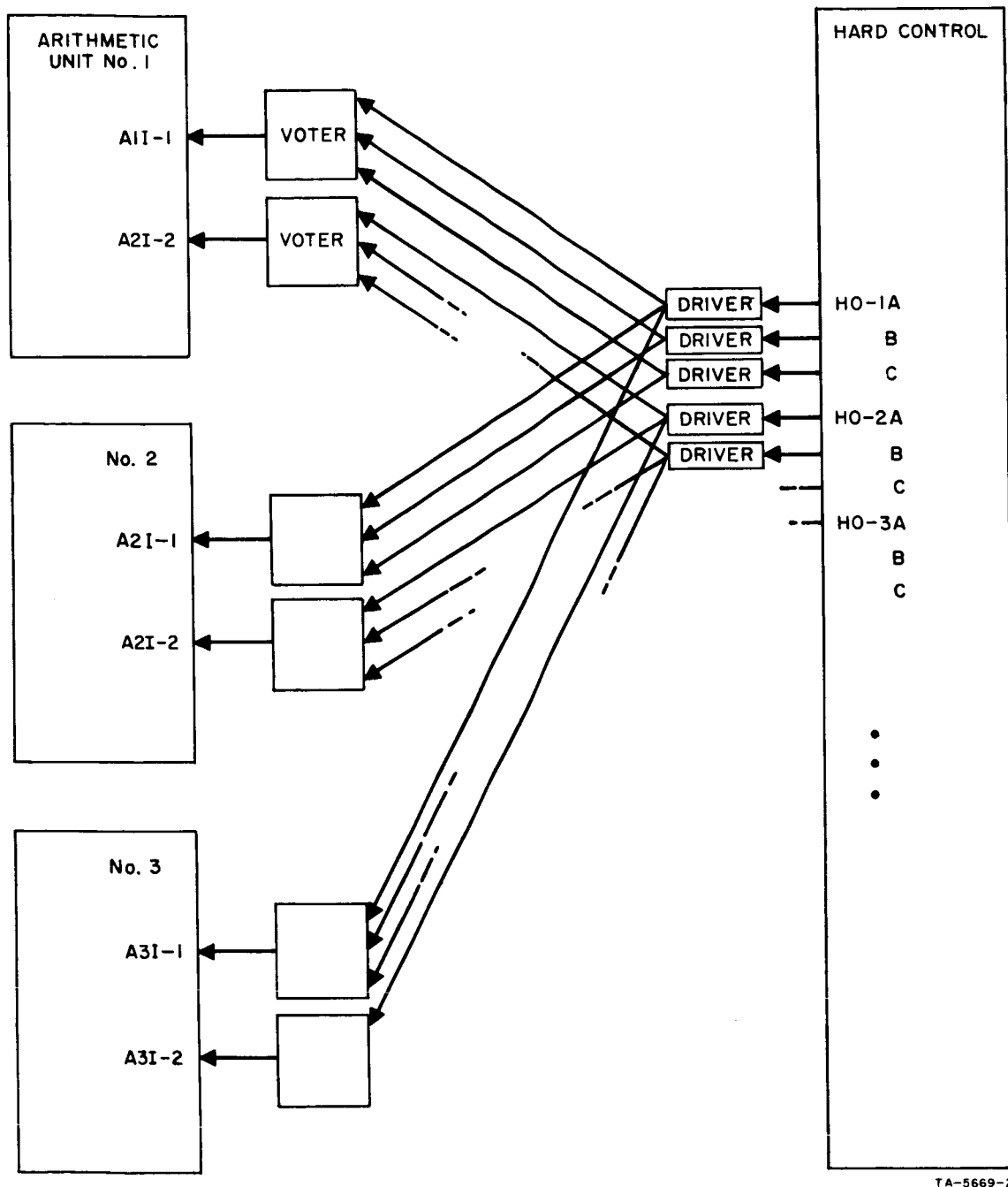
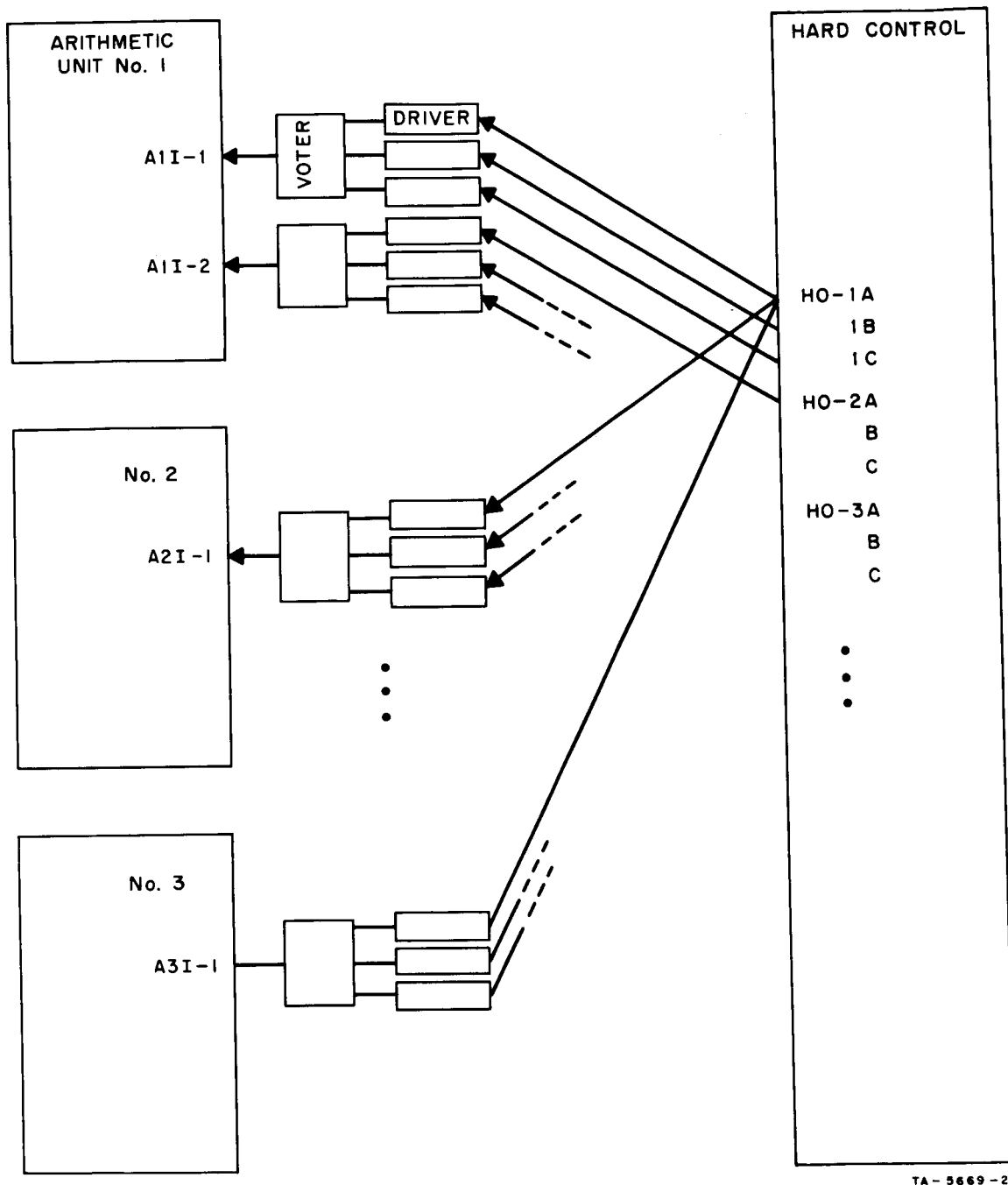


FIG. 21 PARTIAL BLOCK DIAGRAM OF MULTIPLE-VOTER DISTRIBUTOR

voter circuits instead of one. If the second alternative described above is taken, then each set of drivers drives only one voting circuit. The circuit operation is the same as for the Single-Voter Distributor and will not be described again here. The Multiple-Voter Distributor

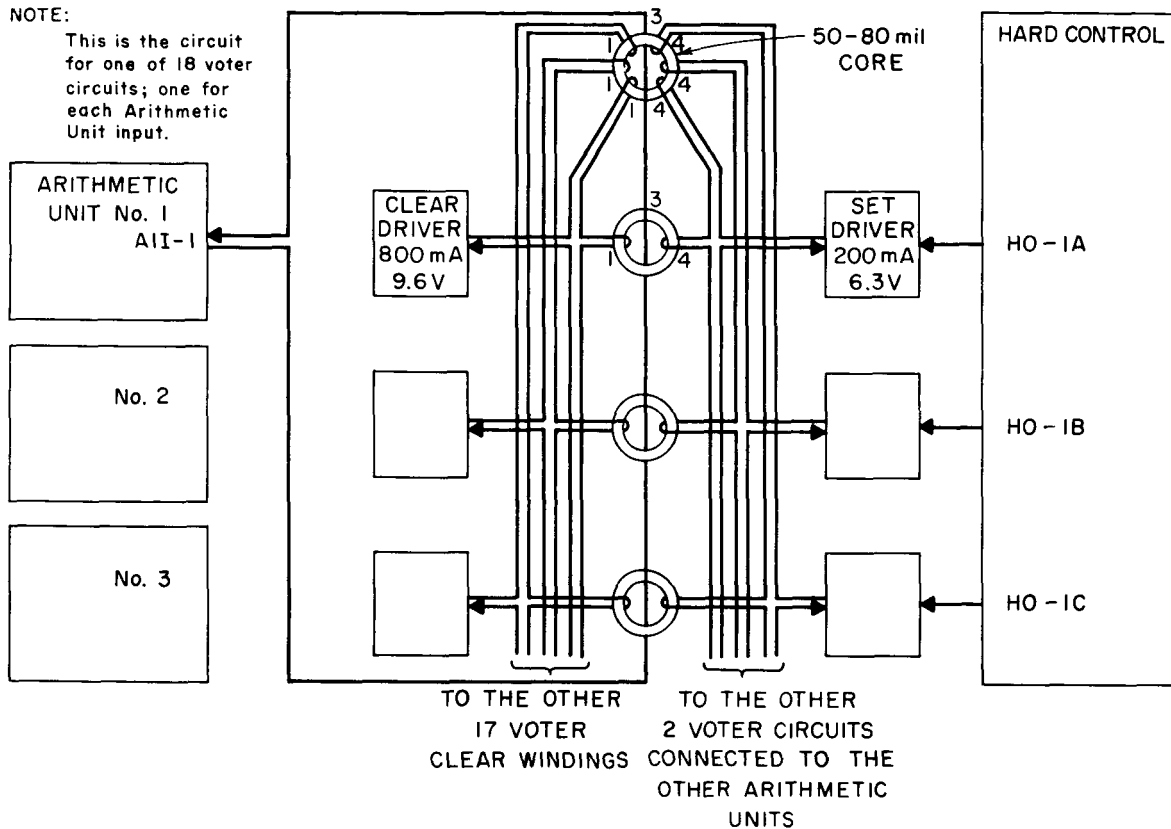


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FIG. 22 PARTIAL BLOCK DIAGRAM OF MULTIPLE-DRIVER DISTRIBUTOR

has 18 voting circuits and 18 drivers. The numbers of cores, turns per core, etc., are shown in Tables VI and VII.

A third alternative, which increases reliability, is to insert isolating transformers ahead of the drivers so that the drivers would



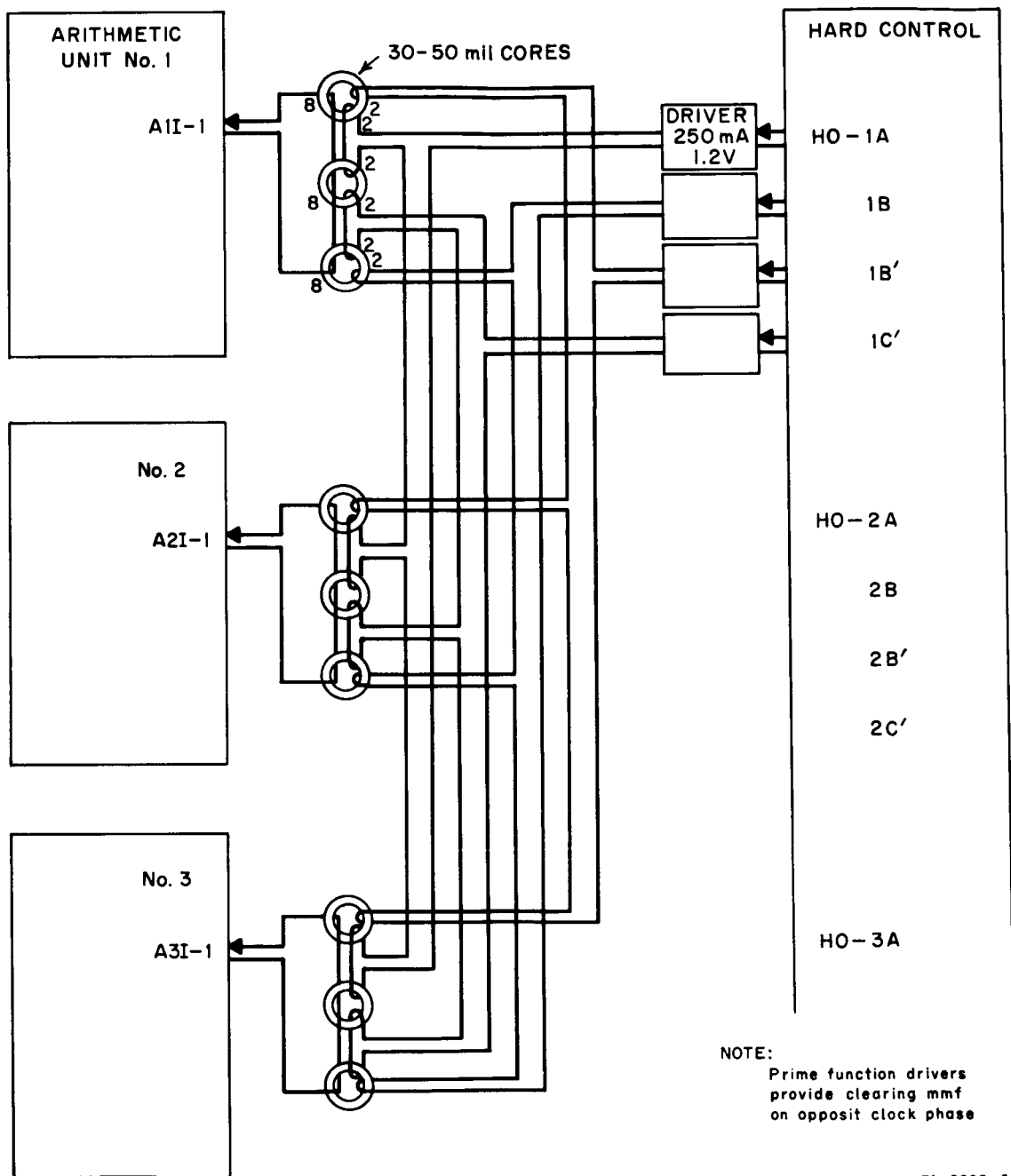
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FIG. 23 SCHEMATIC DIAGRAM OF MULTIPLE-VOTER DISTRIBUTOR

be isolated from each other. This circuit would tolerate a short on an input to one driver without affecting any others. These transformers could be driven directly from MECL NOR circuits.

D. Inhibit Core Voter

This voting circuit can be used as an alternative to the voting circuit used in the Single or Multiple-Voter Distributors described above. The schematic diagram for this voter is shown in Fig. 24. It is shown for the Multiple-Voter case but can be used as well in the Single Voter case. This circuit accomplishes the voting function through generating the necessary AND and OR functions. Each core is driven in such a way as to form the AND function of the two outputs of the Hard Control to which it is connected. One output is connected directly to the core in the set direction. The prime of the other



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FIG. 24 SCHEMATIC DIAGRAM OF INHIBIT-CORE DISTRIBUTOR

output is connected so as to hold the core in the clear direction. The three AND functions generated by the three cores are linked by a single wire to form the OR function necessary to complete the voting operation. The numbers of components, drivers, etc. are shown in Tables VI and VII for comparison with the other alternatives.

E. Comparison of Distributors

The values shown in Tables VI and VII were obtained under the assumption that 50-80-mil memory cores would be used in the cancel type voter circuits. Use of the 30-50-mil core might be practical, in which case the power would be reduced to about 1/3 of that shown in the table. The space would not be significantly reduced since it is the drivers and the terminations that take up most of the space.

The number of solder connections are based on a single wire threading through more than one core. More points would be needed if the windings of each core were soldered to intermediate terminations.

The temperature range estimate is somewhat arbitrary because it is so dependent upon other things. The temperature range is ultimately limited by the Curie temperature of the core materials (around 230°C), but wire insulation becomes a problem and elastic flux increases, which increases the general noise problem, before this temperature is reached.

The fanout capability is unlimited in the sense that drivers and magnetic voting circuits can always be designed to carry any reasonable fanout load at the cost of more space and power.

The maximum speed is not a well-defined limitation on the Distributor circuit. The faster the pulse-repetition rate, the more power and heat there is to contend with. The goal of one megacycle is reasonable, though the cost in power dissipation is high.

The voltage and current requirements can be traded within limits by varying the number of turns on the primary of the voter cores. From the driver point of view it would be desirable to increase turns, but from the power point of view (through use of a smaller core and fewer turns), and the reliability point of view, fewer turns would be desirable.

Core tolerances are not critical since it is saturation that is the crucial characteristic in these circuits rather than magnitude of threshold. The flux capacity of the cores is important in that it must not vary too much between cores, or noise will be introduced. The fact that the magnitude of the saturation flux changes with temperature is not a problem since all the cores will change together.

There is a choice to make between bipolar drivers versus separate clear drivers. The clear drivers were specified here because three separate clear drivers require less additional circuitry than making all 18 set drivers bipolar. The clearing of the cores in the inhibit-type voters is accomplished by driving the prime function drivers with every intermediate phase clock pulse. Thus a unipolar driver can be used and no clear drivers are needed.

The two most significant factors in comparing the Single- and Multiple-Voter Distributors are that all of the magnetic circuits in the Multiple-Voter version are protected with redundancy, and 50 to 75% more cores are required in the Multiple-Voter version to achieve the redundancy.

The added reliability of redundant magnetic circuits would seem well worth the cost of the additional cores.

VII INTEGRATED SEMICONDUCTOR VERSION OF CONNECTION SWITCH

One Cyclic Collector switch and one Distributor Switch will be described. The aim here is to go far enough in the design of a straightforward switch to make a meaningful comparison with an appropriate magnetic version. MECL logic blocks will be assumed as the type of component to be used in these switches.

A. Cyclic Collector

The Block Diagram for the Cyclic Collection is shown in Fig. 25. The switch requires a three-position shift register, 54 two-input AND gates followed by 18 three-input OR gates. Two NAND gates are contained in one integrated circuit module (MECL No. 360). Only one 3-input OR gate can be contained in one integrated circuit Module (MECL No. 356). This gives a total of 45 modules for the AND and OR gates.

The shift registers require one flip-flop module (MECL No. 358) and one dual 2-input NOR per stage. Three registers of four or five stages each require 24 to 30 modules.

The total for the Cyclic Collector Switch is 69 to 75.

B. Distributor

The block diagram for the Distributor shown in Fig. 21, will be used for reference here. The drivers shown on the outputs of the Hard Control are not required for the integrated semiconductor version. Each voter circuit is made up of three 2-input AND gates feeding into one 3-input OR gate as shown in Fig. 26. Six voter circuits are required for each Arithmetic Unit, giving a total of 54 2-input AND gates and 18 3-input OR gates. This is the same number of AND and OR gates required by the Cyclic Collector Switch. The number of modules required is 45 as before.

The total number of modules required for both the Collector and Distributor Switch is from 114 to 120.

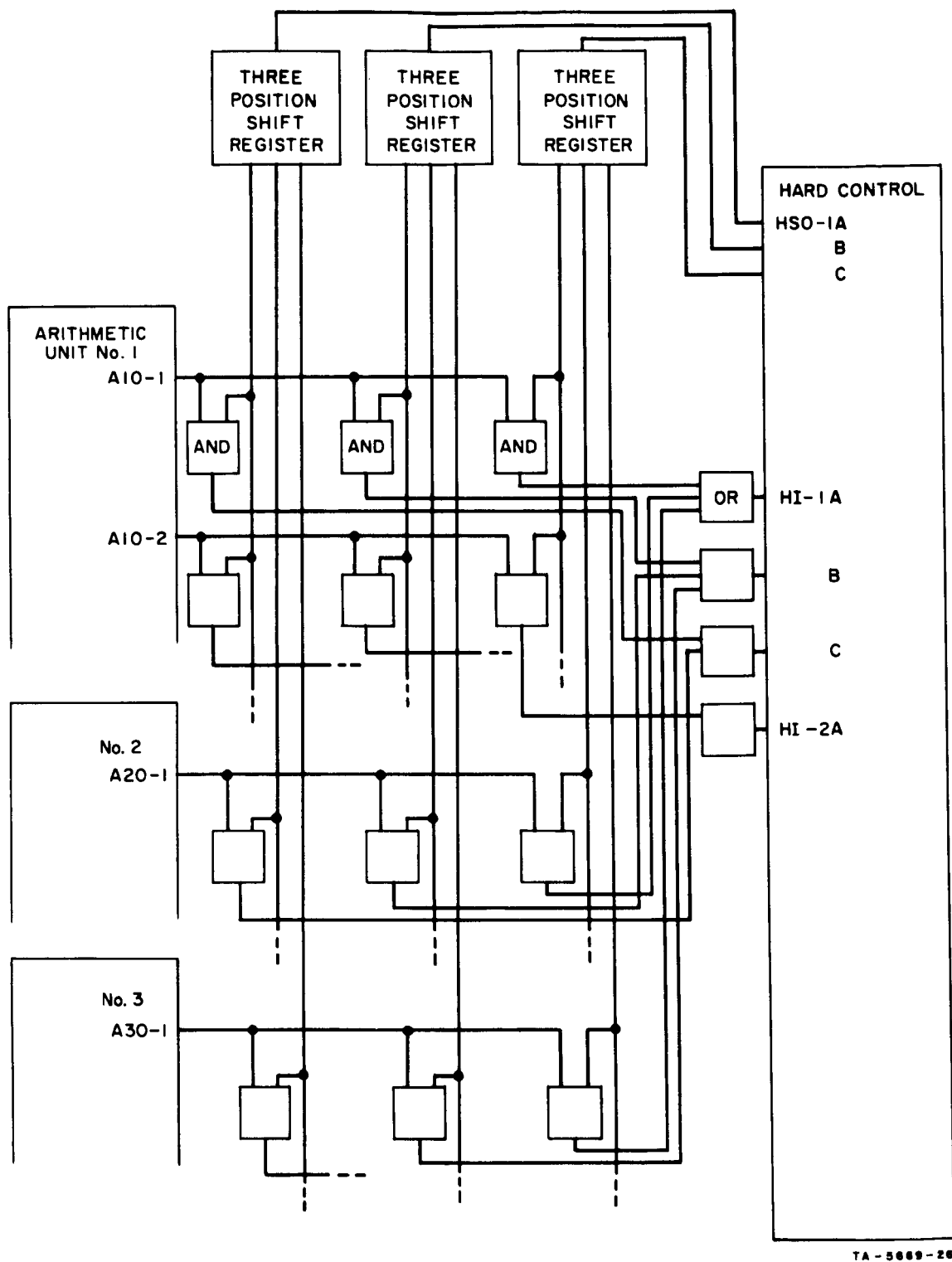
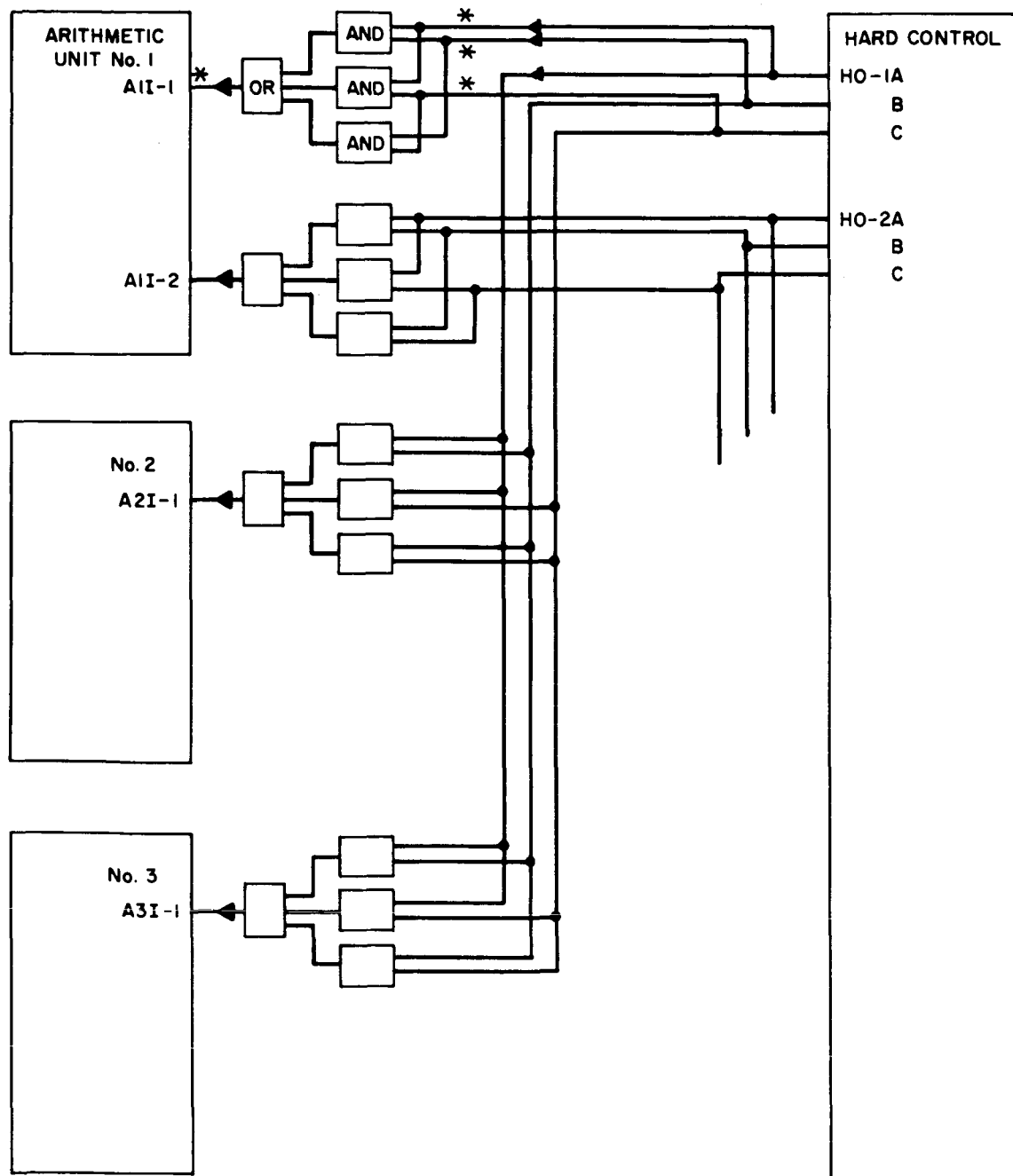


FIG. 25 PARTIAL BLOCK DIAGRAM OF INTEGRATED SEMICONDUCTOR COLLECTOR



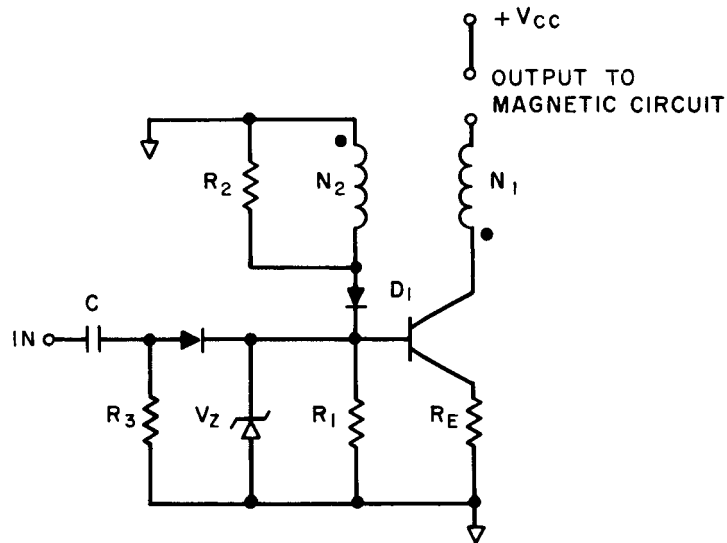
* ISOLATION TRANSFORMERS CAN BE INSERTED EITHER AT THE 3 INPUTS OR THE ONE OUTPUT OF THE VOTER CIRCUITS.

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FIG. 26 PARTIAL BLOCK DIAGRAM OF INTEGRATED SEMICONDUCTOR DISTRIBUTOR

VIII DRIVER CIRCUITS

The majority of the current driver circuits used for the magnetic interconnection switch are of the general type shown in Fig. 27, the



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FIG. 27 DRIVER CIRCUIT

exception being the prime current driver for the shift registers. Basically the circuit consists of a blocking oscillator with a resistance, R_E , placed in the emitter circuit. When the circuit is triggered into its astable state, through the input capacitor, the voltage that builds up on the secondary of the transformer is limited to V_Z volts by the zener diode in the base circuit. The transistor attempts to keep the emitter voltage at V_Z volts, which results in a constant emitter and collector current that is approximately equal to V_Z/R_E . The oscillator reverts to its stable state when the transformer can no longer supply sufficient current to maintain the base voltage at V_Z . In order to make the above description of the circuit operation clear the circuit has been drawn using a positive supply voltage. In practice, where minus supply voltages are available, the supply and

ground terminals are interchanged. The basic reasons for using a blocking oscillator type circuit include: fast rise and fall times, low number of components, and sufficient sensitivity to be triggered directly from MECL logic.

As with any circuit that operates at relatively high current levels and that is driven by a relatively small input swing, care must be taken in circuit layout, especially the ground busses, in order to minimize the possibility of false triggering. It is anticipated that the circuit will have an input discrimination range of at least 0.4 volts over the complete temperature range.

The current and voltage requirements of the magnetic circuits imply a fixed minimum power drain--namely the product of the current through the device, the voltage across the device, and the fraction of the time that the current is being driven through the device. The actual power drawn is the same expression, with the voltage across the device being replaced by the supply voltage. Therefore, in order to minimize the power dissipation the power supply voltage should approach the voltage required by the magnetic device. The supply voltage, however, must be at least equal to the supply voltage plus the sum of the voltage drops across the blocking oscillator transformer, the transistor, and the emitter resistor R_E . The circuit design problem is simplified as the sum of these voltages is increased. Since power dissipation is also increased, a practical minimum of 5 volts for this sum has been set.

Another version of the circuit was considered that used an additional transistor. This circuit would allow the use of lower supply voltages and therefore lower power dissipation. In order to minimize the number of active devices the decision was made to use the one transistor circuit.

The system that uses the magnetic interconnection switch has available both minus-5-volt and minus-20-volt supplies. Since the voltage drop in the blocking oscillator circuit alone is 5 volts, the minus-20-volt supply must be used. Increasing the turns on the magnetic

device it is possible to decrease the amount of current required. There is an associated increase in the amount of voltage across the device. By adjusting turns it is possible to "match" the magnetic device to the supply voltage.

The register prime driver circuit will consist of a timing circuit, a voltage ramp generator, and a current driver circuit. The timing circuit will be either a one-shot or blocking oscillator. The estimated parts count for this circuit is given in Table VIII.

Table VIII shows the peak and average power dissipations for the total driver circuit and the driver transistor used to drive each of the magnetic circuits. It is clear that in space environments care will have to be taken in order to insure a heat flow away from the transistors and other circuit components. Although transistors of moderate power capacity and price were used in the preliminary phase, for future, more critical applications, transistors are available that would operate at a lower power level relative to their maximum power rating.

Table VIII
DRIVER COMPONENT COUNTS AND PERFORMANCE ESTIMATES

	Pulse Width (μ s)	Peak Pulse Current (A)	Mag. Crt. Voltage Drop (V)	No. of Turns	Average Power (W)	Peak Power (W)	Average Transistor Power (W)	Peak Transistor Power (W)	No. of Transistors	No. of Resistors	No. of Capacitors	No. of Diodes	No. of Transformers	No. of Solder Joints
Register Advance	1	5	12	-	Low	100	Low	10	1	4	1	3	1	23
Register Prime	200	.55	1.1	-	Low	10	Low	5	5	10	3	5	0	51
Minor Aperture Set	.3	.2	12	3	1.2	4	.24	.8	1	4	1	3	1	23
Minor Aperture Clear	.5	.4	12	1	4	8	.98	1.6	1	4	1	3	1	23
Cancel Voter (Single) 50-80 Set	.3	.2	2.1	4	1.2	4	.24	.8	1	4	1	3	1	23
Cancel Voter (Single) 50-80 Clear	.3	.4	6.3	2	2.4	8	.48	1.6	1	4	1	3	1	23
Cancel Voter (Multiple) 50-80 Set	.3	.2	6.3	4	1.2	4	.24	.8	1	4	1	3	1	23
Cancel Voter (Multiple) 50-80 Clear	.3	.8	10	1	7.8	16	.96	3.2	1	4	1	3	1	23
Cancel Voter (Multiple) 30-50 Set	.3	.25	2.4	2	1.5	5	.3	1	1	4	1	3	1	23
Cancel Voter (Multiple) 30-50 Clear	.3	.25	7.2	1	1.5	5	.3	1	1	4	1	3	1	23
Inhibit Voter (Multiple) 30-50	.3	.25	1.2	2	1.5	5	.3	1	1	4	1	3	1	23

Notes: (1) Current waveform is a damped sine wave with 1.5 μ s rise and 3.5 μ s fall times
(2) Current waveform is a ramp taking 100 μ sec to reach peak value and exponential fall with $\gamma = 70 \mu$ s.

IX COMPARISON OF CONNECTION SWITCH ALTERNATIVES

A. General

The choice of a shift register circuit for the cyclic switch was made on the basis of the temperature range requirement, reliability requirement, and the fact that speed of shifting was not important. Where speed is not important and wide temperature range is desired, the MAD-R shift register is significantly better than the competing techniques of Flux Doubling and Balanced Magnetic circuits.

The other functions involved in the switch are simple, in that no sequence of operations is required, but only single operations, such as gating and voting. General magnetic logic techniques are not required for these simple functions and would require more circuitry than the simple approaches described in the preceding sections.

The comparisons to be made below are primarily comparisons between the alternatives of redundant versus nonredundant magnetic circuits and secondarily between circuit types. Comparison of the magnetic versions with an integrated semiconductor version of the switch is made also.

B. Collector Alternatives

A comparison of the selector with the cyclic type Collector shows that the selector type is a basically more simple circuit, but it gains this simplicity by shifting the burden of memory of switch position on to the Hard Control. It has become clear in the course of the project that it is more appropriate to have the switch position memory in the switch itself rather than in the Hard Control. On this basis the Cyclic switch alternatives are considered here rather than the selector.

Performance data and component counts for the two alternative Cyclic Collector switches are given in Tables II and III. Two methods of fanout to the three redundant channels of the Hard Control are shown in Fig. 9. The method using cores rather than resistors is assumed here because it provides better isolation and reliability.

The most significant factor in the difference in performance between the redundant and nonredundant versions of the cyclic switch is that coupling loops are involved in the voting and fanout circuits in the nonredundant but not in the redundant version. The voter circuit coupling loops driving the register represent low-impedance loads on the drive lines, which cause interaction between the drive lines that are being driven and those that are not, as explained in Sec. III-G-3. This interaction tends to diminish drive pulse ranges generally, to some extent, and requires some degree of temperature tracking of the prime current amplitude to achieve the desired temperature range.

The coupling loop required for fanout creates a potential noise problem if linear material is used in the fanout cores, because the collapse of the flux in the fanout cores after clearing the information apertures of the registers tends to induce a voltage that is in a direction to spuriously switch the input circuits to the Hard Control. Linear material rather than square loop is preferable for the fanout cores because they require less drive current.

The advantages of each alternative are listed below:

Redundant Version

- (1) Better performance
- (2) Higher reliability (due to redundancy in the magnetic circuitry)
- (3) Slightly lower current required from register drivers.

Nonredundant Version

- (1) One-third the number of multiaperture cores, and somewhat fewer total number of cores
- (2) Probably lower fabrication cost

The redundant version appears to be the better choice.

C. Distributor Alternatives

In this case, as in the case of the Collector, the primary comparison is between redundant (Multiple-Voter) and nonredundant (Single-Voter) circuits. The circuit that is made redundant is a voting circuit, but switched redundancy is the technique involved since failure in a voting circuit has the same overall effect on the operation of the computer as a failure in the corresponding arithmetic unit. The drivers, however, are protected with voting redundancy since they are connected directly to the redundant channels of the Hard Control and the magnetic voters.

The comparison of the two alternatives here is more clear-cut than in the case of the Collector. It is simply a question of whether or not it is worth 50 to 75% more magnetic circuitry to achieve the gain in reliability that results from making the magnetic circuitry redundant. The number of drivers is the same in each case. The coupling loop does not cause the deterioration in performance that it did in the Collector because there is no drive-line interaction problem here. The problem of noise during the clearing of the voter cores, where linear fanout cores are used, can be solved using square-loop cores if necessary without significant deterioration of performance.

There is a choice between the Cancel and the Inhibit type of voter circuit which is independent of the choice between redundant and non-redundant magnetic circuits. The Inhibit type requires 15 percent more drivers and the Cancel type requires 30 percent more cores. The choice between these two types of voting circuits should be made after their performance is thoroughly checked out in the laboratory.

D. Recommended Alternatives

The recommendations made here relate only to the magnetic versions of the switch. The integrated semiconductor version is considered relative to the magnetic versions in Sec. VIII-E below. Magnetic versions in general, rather than specific ones, are considered in that section because the most significant aspect of the comparison related to the drivers of the magnetic circuits rather than the magnetic circuits themselves.

Specific circuits are recommended for the magnetic version of the switch, but only the pertinent information is given for evaluating the integrated circuit version relative to the magnetic version.

For the Collector, the Cyclic type is specifically recommended over the Selector type primarily because it maintains its position when power is off.

The redundant Cyclic Collector is recommended over the Nonredundant Cyclic Collector primarily because of superior performance. This version is described in detail in Secs. III-B, III-D, and III-E. Summary data is given in Table IX.

For the Distributor, the Multiple-Voter type is recommended over the Single-Voter type on the basis of higher reliability. This circuit is described in detail in Sec. VI-C and in Tables VI and VII.

No specific recommendation is made relative to the Cancel versus the Inhibit type voting circuit for the Distributor because there is no significant difference in their performance as far as can be determined at this point. Since the circuits are quite simple, they should both be analyzed and tested thoroughly before one is selected. The summary data in Table IX is based on the Inhibit type circuit.

E. Magnetic Versus Integrated Semiconductor Versions

The number of transistors in the driver circuits for the magnetic versions of the switch is a crucial factor in comparing the reliability of the magnetic version with that of the integrated semiconductor version. Even though preliminary circuit design and breadboard work have been done, indicating that the information drivers can be made with just one transistor in each driver, two transistors each is still considered a possibility because, when a thorough analysis is made, it may be found that stable, reliable operation with adequate noise discrimination cannot be achieved with just one transistor per driver. If an adequate information driver could be made with one transistor, the number of transistors in the drivers would be of the order of half the number of integrated circuit modules required for the integrated

Table IX

SUMMARY OF COMPONENT COUNTS AND PERFORMANCE ESTIMATES

	Number of Components				
	Redundant Cyclic Collector	Multiple- Voter Distributor	Both Collector and Distributor	Three Magnetic Switches	Three Integrated Circuit Switches
Total Cores	72	54	126	378	--
Total Turns	600	648	1248	3744	--
Total Drivers	30	24	54	162	
Total Transistors	48 to 69	24 to 28	72 to 117	216 to 351	--
Total Integrated Circuit Modules					342
Total Peak Power ¹ (Watts)	34	36	70	210	20
Total Average Power ² (Watts)	23	36	59	177	20
Total Volume (cu. in.)	47	35	82	246	135

Temperature Range-- -10°C to $+85^{\circ}\text{C}$

Clock Rate--1 Mc/s

¹For all one's in information channels.

²For alternate one's and zero's in information channels.

circuit version of the switch. If two were required, the number of transistors and integrated semiconductor modules would be close to equal, as indicated in Table IX.

Power consumption of the magnetic version is inevitably high for a clock rate of one megacycle per second. It is estimated to be about an order of magnitude higher than the integrated circuit version. Standby power is very low and can be made essentially zero by turning off the clock to the clear drivers under standby conditions.

The volume of the magnetic version is about twice that of the integrated semiconductor version primarily because of the discrete component realization of the driver circuitry. If all of the circuitry except the output transistor were made into an integrated circuit module, the volumes of the two versions would be approximately equal.

Isolation and switch position memory are provided in the magnetic version, but not in the integrated semiconductor version. It is apparent that isolation can be achieved with pulse transformers that can be driven directly with integrated semiconductors, but switch position memory cannot be so easily achieved. It is possible to arrange the Hard Control so that the core memory could be used to remember the switch position through a power failure, but it would seem more appropriate to have the nonvolatile position memory in the switch itself. There are undoubtedly a number of ways of combining magnetics and semiconductors to achieve this memory capability, one of which is a magnetic shift register that might or might not incorporate the gating within the shift register core structure.

For an information rate of 1 Mc/s and using the available power supply levels, the magnetic switch requires about an order of magnitude more power than the integrated semiconductor version.

The choice here is not necessarily between using magnetic circuits exclusively or integrated semiconductors exclusively. The Collector could use magnetic circuits and the Distributor integrated semiconductors, or the Collector could use both kinds of circuits. A combination of the two types of circuits in the Distributor does not appear to be as appropriate as in the Collector.